PICREF-2 REFERENCE DESIGN

Intelligent Battery Charger

PICREF-1

Uninterruptible Power Supply Reference Design

INTRODUCTION

At times, power from a wall socket is neither clean nor uninterruptible. Many abnormalities such as blackouts, brownouts, spikes, surges, and noise can occur. Under the best conditions, power interruptions can be an inconvenience. At their worst, they can cause loss of data in computer systems or damage to electronic equipment.

It is the function of an Uninterruptible Power Supply (UPS) to act as a buffer and provide clean, reliable power to vulnerable electronic equipment. The basic concept of a UPS is to store energy during normal operation (through battery charging) and release energy (through DC to AC conversion) during a power failure.

UPS systems are traditionally designed using analog components. Today these systems can integrate a microcontroller with AC sine wave generation, offering the many benefits listed below.

PIC17C43 Microcontroller Benefits

- High Quality Sine Wave - High throughput allows for high quality output
- Flexibility - core control features and operations can be changed with software modifications only
- Transportability of Design
- Variable Loop Response
- Digital Filtering
- Parts and Complexity Reduction
- Peripheral Integration
- Ease of Interfacing
- Testability
- Time to Market

PICREF-1 OVERVIEW

The Microchip Technology PICREF-1 UPS Reference Design offers a ready-made uninterruptible power supply solution with the flexibility of a microcontroller.

The PIC17C43 microcontroller handles all the control of the UPS system. The PIC17C43 is unique because it provides a high performance and low cost solution not found in other microcontrollers.

The PIC17C43 PWM controls an inverter whose output, when filtered, results in a sinusoidal AC output waveform. Fault signaling can be initiated internal or external to the PIC17C43 depending on the type of fault. A fault will disable the entire inverter. The output voltage and current will be monitored by the PIC17C43 to make adjustments “real-time” to correct for DC offset and load changes.

The PIC17C43 controls all module synchronization as well as inverter control and feedback. The PIC17C43 uses zero crossing for synchronization of input voltage/phase to output voltage/phase. All internal module synchronization is handled by the PIC17C43.

The control algorithms and software are written in C for maintainability and transportability.

PICREF-1 Key Features

- True UPS Topology
- True Sinusoidal Output
- Point-to-Point Output Correction
- 1400 VA Rating
- 120/240 V Input

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SYSTEM OVERVIEW

The power flow for the PICREF-1 system is shown in Figure 1. The Uninterruptible Power Supply (UPS) is either supplying power based on the input power, if the unit is plugged in, or based on the batteries.

Power Flow

When available, the input power is filtered for common mode noise and is protected from surges/spikes by input power protection circuitry. The power then goes into the power factor correction (PFC) module which forces the input current to be sinusoidal so that power utilization is more efficient. The PFC module also rectifies the input AC power to produce voltage-regulated DC power which is used by the rest of the functional modules.

This rectified AC power is OR'd through diodes with the DC voltage generated from the battery boost circuit. The battery boost voltage is set slightly lower than the rectified AC input voltage so that, under normal conditions, the rectified AC input power provides power to the load. Once the voltage from the rectified AC input source drops below the battery boost DC voltage, the power is drawn from the battery boost module. In this mode the battery charger is turned off so as not to cause an additional load on the battery (i.e., so the battery is not charging itself).

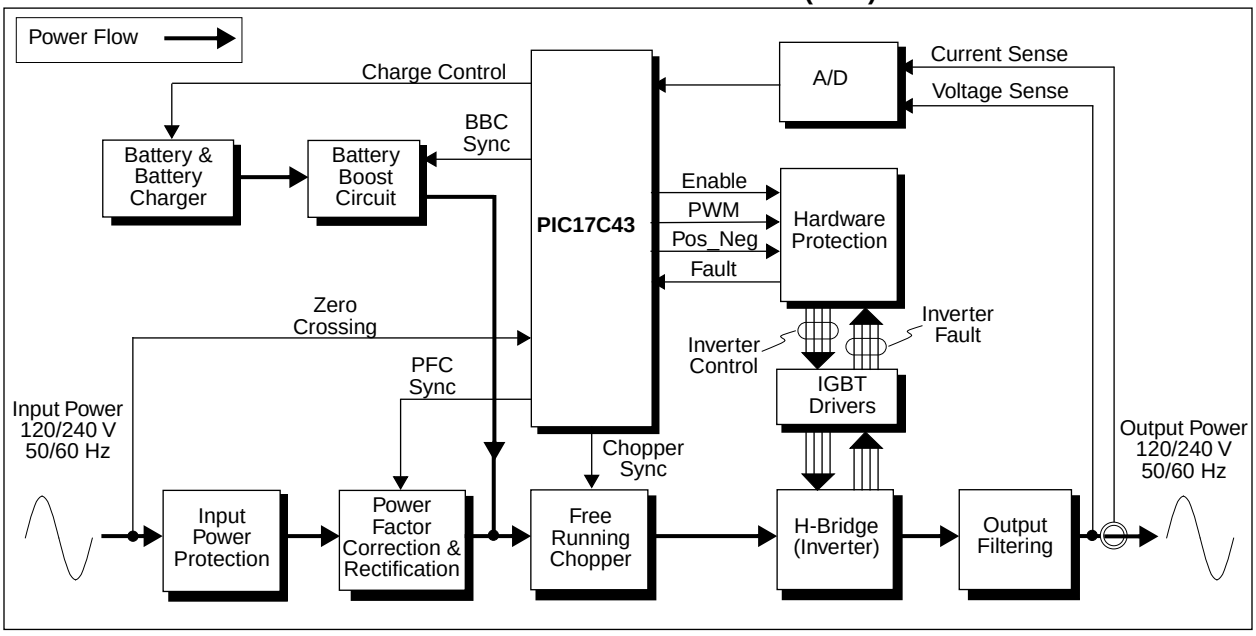
The OR'd DC bus voltage is fed into the free running chopper which both isolates the DC bus from the H-Bridge inverter and doubles the DC voltage for the inverter to operate at 120 or 240 volts. The output of the chopper is filtered to remove switching noise and then fed into the H-Bridge.

The PIC17C43 microcontroller controls the inverter by driving the H-bridge through Hardware Protection circuitry and Insulated Gated Bipolar Transistor (IGBT) drivers. The output of the H-bridge is filtered and drives the load with an AC sine wave that is synchronized to the input AC voltage.

An A/D converter provides feedback to the PIC17C43 for output monitoring.

All module synchronization, control, and fault detection are handled through the PIC17C43.

FIGURE 1: PICREF-1 UNINTERRUPTIBLE POWER SUPPLY (UPS) BLOCK DIAGRAM



Inverter Operation

The H-bridge circuit works by generating the separate positive and negative cycles needed for sine wave generation. The PIC17C43 controls all signals to the hardware protection circuitry and IGBT drivers and thus controls the generation of the sine wave (Figure 2).

Software Fault / No Enable

Driving the FAULT HIGH will disable the inverter's power stage.

Hardware Fault

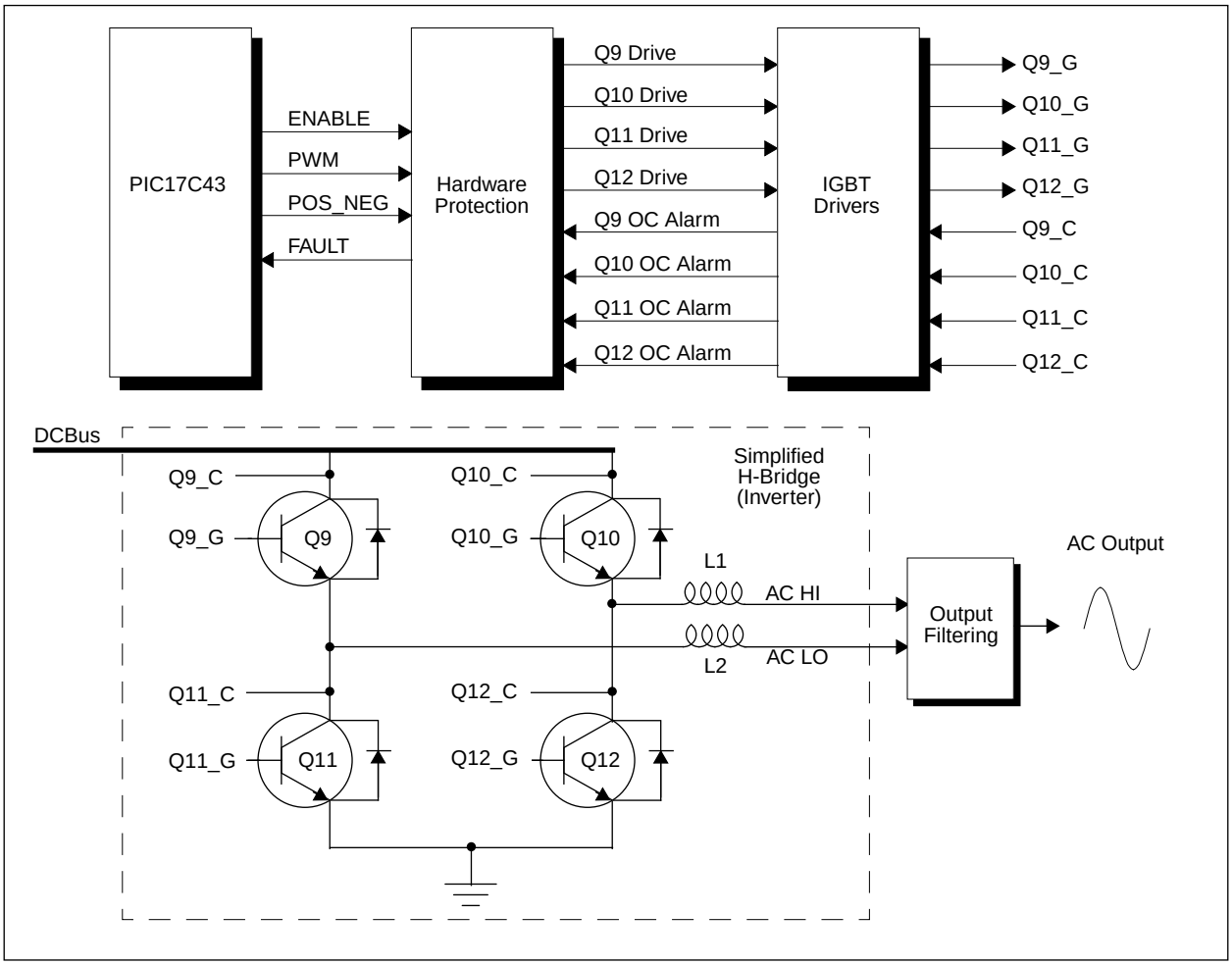
The hardware protection logic automatically disables the inverter's power stage in the event any of the IGBT's have gone out of saturation, i.e., an external short was placed on the H-Bridge which was so severe that an appreciable voltage was developed across one of the switches that was on. This feature prevents a short from immediately destroying the switching devices.

As long as none of the out-of-saturation signals (Q9/Q10/Q11/Q12 OC Alarm) are LOW, the power stage can be enabled. When the PIC17C43 is first powered up, the ENABLE line (PORTC, bit0) will be in a high impedance state. A pull-down resistor keeps the ENABLE line held LOW so that any spurious signals which may be generated while the system is initializing will not drive the H-Bridge. If any of the out-of-saturation signals go LOW, the FAULT signal goes HIGH, reporting to the PIC17C43 that an external fault occurred. This will disable the H-Bridge.

The inverter may be re-enabled by cycling the ENABLE line LOW and then HIGH to reset the flip-flop and allow the PIC17C43 to drive the H-Bridge again.

The PIC17C43 microcontroller and hardware protection circuits are found on the PICREF-1 Inverter Control Card. IGBT driver circuits are found on the Inverter Drive Card. Schematics for these cards can be found in Appendix B.

FIGURE 2: INVERTER OPERATION



Normal Operation

In normal operation (FAULT is LOW and ENABLE is HIGH), the states of Q9, Q10, Q11 and Q12 are determined by POS_NEG and PWM signals. These signals pass through steering logic which produce transistor (QX) drive signals (see Inverter Control Card schematics in Appendix B).

The steering logic causes the IGBT pairs Q9,Q11 and Q10,Q12 to be held in the OFF state for one microsecond before allowing them to switch ON. This prevents shoot-through from occurring during changes of states from the PWM. This is necessary because of the relatively slow turn off times for the IGBTs. This prevents complementary pairs from being ON at the same time.

Table 1 describes the drive values for different input values of POS_NEG and PWM.

TABLE 1 INVERTER CONTROL SIGNALS

POS_NEG	PWM	Q9 Drive	Q10 Drive	Q11 Drive	Q12 Drive
0	0	0	0	1	1
0	1	1	0	0	1
1	0	0	0	1	1
1	1	0	1	1	0

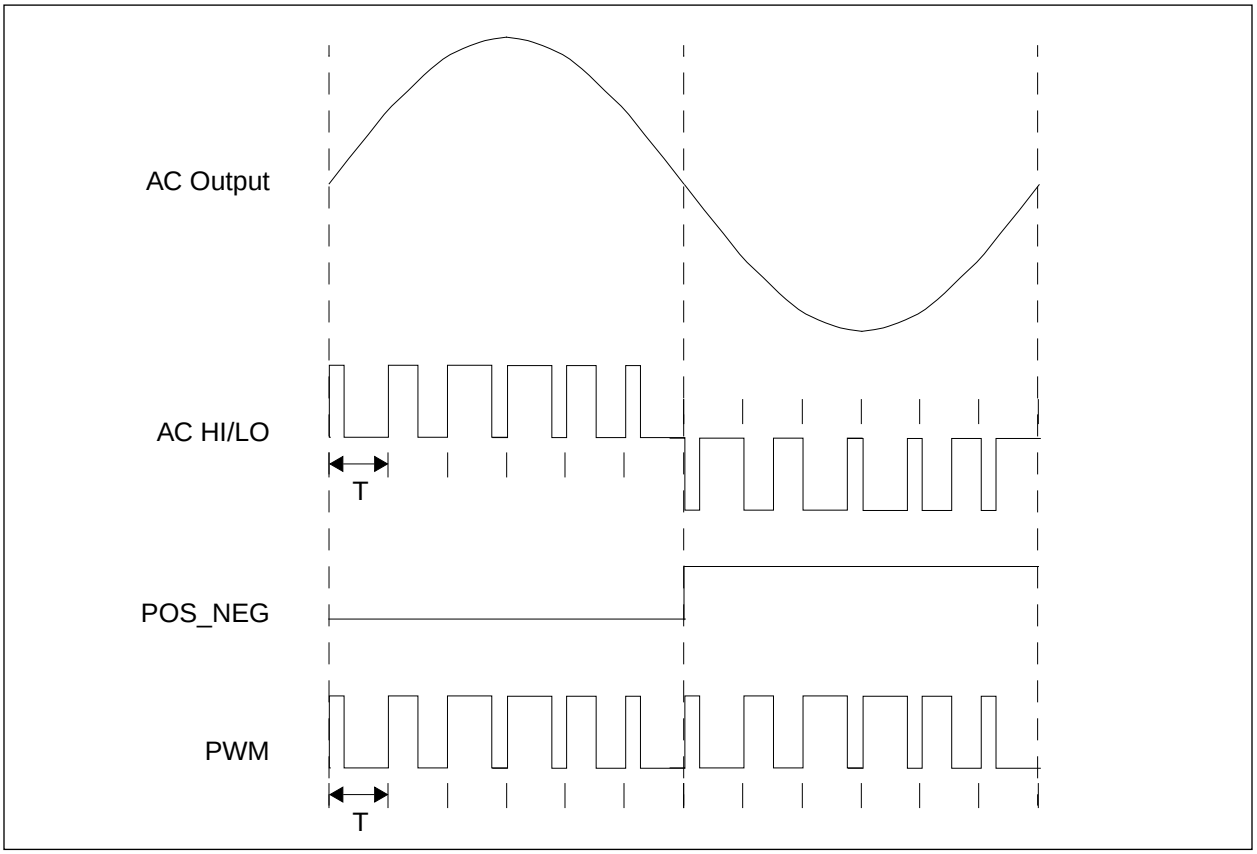
QX Drive = 1 -> transistor QX is OFF
QX Drive = 0 -> transistor QX is ON

The transistor drive signals are fed into the IGBT Drive circuits (Inverter Drive Card) to determine the state (ON or OFF) of each transistor. A drive signal of '1' corresponds to an IGBT being OFF, and a drive signal of '0' corresponds to an IGBT being ON.

From Table 1, when the POS_NEG signal is 0, Q10 is held ON, Q12 is held OFF, and Q9,Q11 are modulated in a complementary fashion with the PWM signal. Similarly, when POS_NEG is 1, Q9 is held ON, Q11 is held OFF, and Q10,Q12 are modulated in a complementary fashion with the PWM signal. Therefore, the differential output signal from the H-Bridge has an average value proportional to the duty cycle of the PWM signal and a polarity set by the POS_NEG signal. The output filter smooths this pulse train and all that remains is the average value of the PWM signal (Figure 3).

To understand how the PIC17C43 determines the modulation for the H-Bridge transistors, please see the section *Software Overview.*

FIGURE 3: INVERTER WAVEFORMS



HARDWARE OVERVIEW

This section describes the PICREF-1 hardware and how it functions in the UPS system. Hardware detail (schematics) may be found in Appendix B.

Microcontroller

A typical analog UPS solution is shown in Figure 5. By using a microcontroller, this design can be greatly simplified. That is, the functions of the DC offset amp, error amp and PWM drive can be implemented in software. Therefore, modifications to the design are made through code changes, not component changes.

In addition, there is no need to generate an external sine wave reference; this is embedded in the microcontroller.

The PIC17C43 is the heart of PICREF-1 (Figure 4). The high performance of the Harvard architecture gives the user the throughput needed for high quality sine wave generation. The single-cycle multiply means faster program execution and response to waveform changes. Only 8 bits of the 10-bit PWM is needed to resolve a high quality output waveform.

In addition, using a PIC17C43 microcontroller enables the customer to use the same core control for multiple products (transportability) and add further enhancements through software changes (flexibility).

Use of the PIC17C43 means the availability of variable loop response, or software that can adjust to different loads. Digital filtering is another microcontroller benefit as it reduces components that would be necessary for analog filtering.

Also, the high level of peripheral integration (from the PIC17C43's USART and PWM modules) further reduces the complexity of the design. This reduces the development time and the components needed.

Converting from analog to digital also enhances the repeatability, manufacturability, and flexibility of the design. Product test is made easier as well, and time-to-market is reduced.

FIGURE 4: PIC17C43 PINOUT

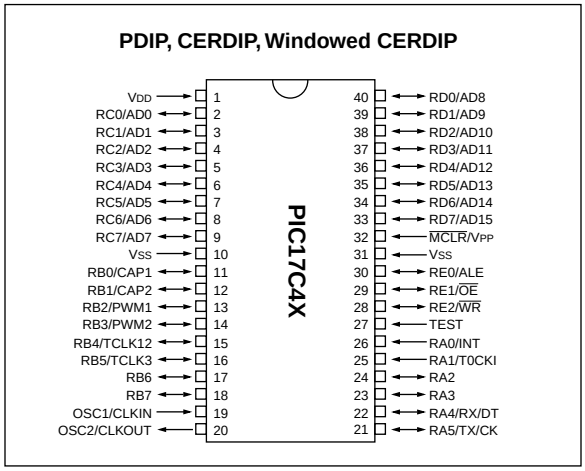
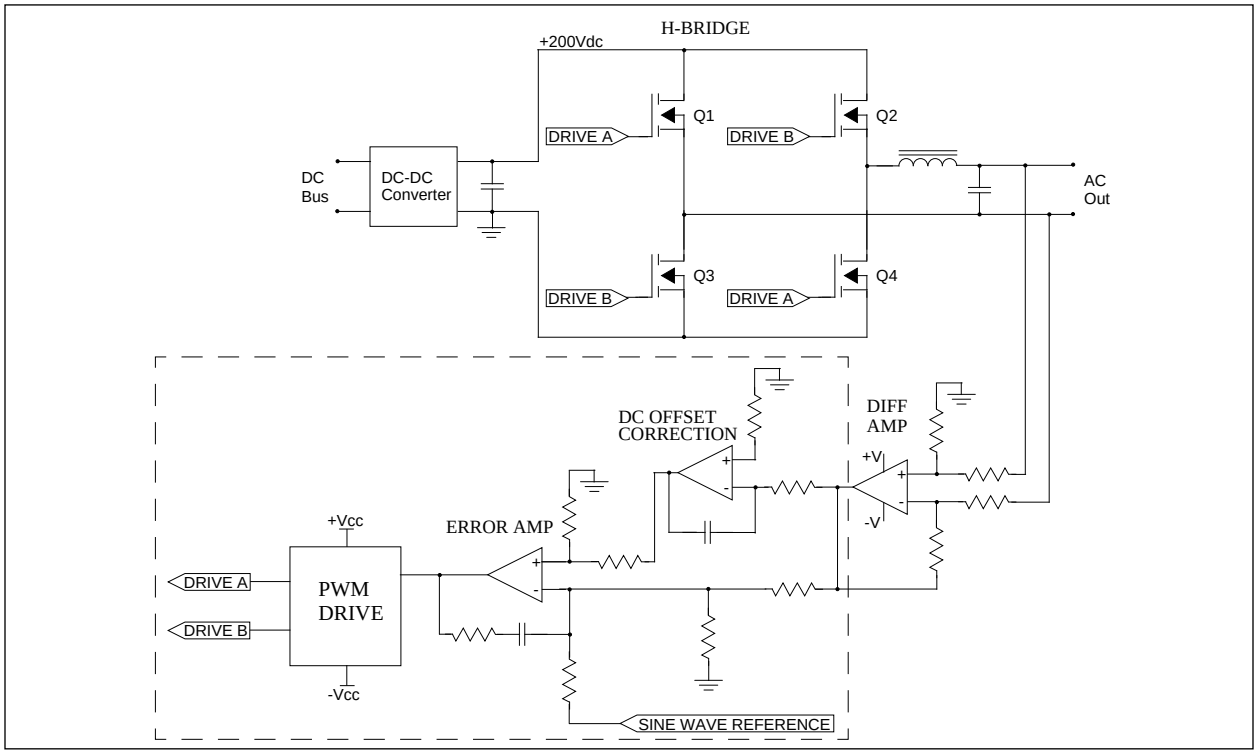


FIGURE 5: TYPICAL ANALOG SOLUTION



Input Power Monitoring

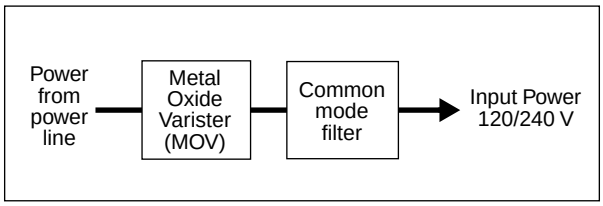
The input power is monitored to determine the value of the output waveform. So, if 120V is input, 120V will be output, and if 240V is input, 240V will be output.

The 120V/240V relay (power switch) shown in the schematics (Appendix B) has not been implemented as this would have been part of the software “housekeeping” functions.

Input Power Protection

The input filtering circuit provides input protection for the UPS and isolation from the power source. The main components of the circuit are the MOV, which suppresses surges/spikes, and the input power line filter. The common mode filter prevents UPS switching noise from getting back onto the main power lines.

FIGURE 6: INPUT FILTERING CIRCUIT



EMI/RFI filtering and spike/surge protection are very important in a robust UPS design. Input filtering is heavily dependent upon design specifics (shielding, grounding, layout, etc.), so following sound design principles and testing is the only way to verify actual performance.

Power Factor Correction & Rectification

This portion of the PICREF-1 has not been implemented. However, the theory of how power factor correction circuitry would function in a UPS is discussed here, and a general PFC schematic is given in Appendix B.

The output from the input filtering circuit feeds into the power factor correction (PFC) circuit. The PFC circuit produces a regulated DC bus by means of a full wave rectifier which feeds a boost converter. The PFC control system consists of two feedback loops. A current loop forces the input current to match the waveshape and phase of the input voltage, thus producing a high power factor. The secondary outer loop adjusts the magnitude of the input current so that the output DC voltage is regulated. This circuit also detects the magnitude of the input voltage. This is used to set the output voltage magnitude.

Synchronization of the PFC is derived from the microcontroller.

PFC comes into play when designing for high power requirement applications. In discussing power requirements for a system, care must be taken in defining terms. In a DC system, the DC source supplies real current to the real load. The power for this system is defined in watts (volts x amps).

By their nature, switched mode power supplies have a reduced power factor. This is due to the fact that the current is delivered in narrow pulses at the peak of the voltage sine wave. This increases the RMS value of current, which limits the current that can be drawn from a typical wall socket. Therefore, with power factor correction, available power increases and distortion decreases.

The example below shows how PFC can increase the ability to drive loads from a typical outlet.

EXAMPLE 1: POWER FACTOR CORRECTION USAGE

The power source is 120 V ±- 10% at 20 Amps with a 20% derating.

The input to the UPS PFC’d to 0.95.

The efficiency of the UPS is 70%.

The load is a workstation which is rated at 900 Watts with a PF of 0.65.

Can the load be driven with a 1400 VA rated UPS and a standard outlet (20A)?

Load Power:

PF = (Pout Watts / Pout VA)

0.65 = 900 W / Pout VA

Pout VA = 1384 VA

Input Power:

Pin Watts = Pout Watts / Efficiency

Pin Watts = 900 Watts / 0.70

Pin Watts = 1286 Watts

Pin Watts = Vin (Min) * Iin * PFC

1286 Watts = 108 V * Iin * 0.95

Iin = 12.5 Amps

Available Current:

20 Amps x 80% = 16 Amps

(VA rating is volts * amps. Power drain is watts. PF is Watts/VA and is typically 0.6-0.7 for computers.)

From the output power perspective, the load power for the workstation is below 1400 VA, so the device can be driven. From the input power perspective, the power need is 1286 watts, which translates into 12.5 Amps of current at the minimum input voltage. The derating of the outlet is 16 Amps, so the outlet is capable of providing the current needed to supply the UPS. However, if the PF at the input would have been 0.65 instead of 0.95, the current required would have been 18.3 Amps which would violate the derating conditions.

Battery, Battery Charger and Battery Boost Circuit

This portion of the PICREF-1 has not been implemented. However, the theory of how a battery back-up circuit (battery, battery charger and battery boost) would function in a UPS is given here.

The battery is charged from input power once the bus voltage exceeds 40V DC. The input power turns off when the bus voltage drops below 40V DC. The battery charger circuit turns off when the battery power is enabled.

The 48V DC battery bus is stepped up to 360V through the battery boost (push-pull) circuit. The battery boost voltage is slightly less than the battery charger bus voltage created from the input power source. This is done so that the power source under normal operation is the input power. A UC3825 PWM controller is used as part of the battery boost control circuitry due to its integrated drive protection and low cost.

The UC3825 is optimized for high frequency switched mode power supply applications. Particular care was given to minimizing propagation delays through the comparators and logic circuitry while maximizing bandwidth and slew rate of the error amplifier. This controller is designed for use in either current mode or voltage mode systems with the capability for input voltage feed-forward.

Protection circuitry includes a current limit comparator with a 1V threshold, a TTL compatible shutdown port, and a soft start pin which will double as maximum duty cycle clamp. The logic is fully latched to provide jitter free operation and prohibit multiple pulses at an output. An under-voltage lockout section with 800mV of hysteresis assures low start up current. During under voltage lockout, the outputs are high impedance.

This device features totem pole outputs designed to source and sink high peak currents from capacitive loads, such as the gate of a power MOSFET. The ON state is designed as a high level.

DC Bus

The 380V DC bus is generated either from the primary power source, under normal operating conditions, or the battery boost circuit, under “no power” conditions. The DC bus is filtered for noise and spikes at the input to the free running chopper.

Free Running Chopper

The free running chopper generates a square wave at twice the magnitude of the DC bus. The frequency of the chopper is 100kHz and the duty cycle of the square wave is approximately 45%. A current transformer is used for sensing the current. A UC3825 PWM controller is used due to its high PWM frequency and low cost.

The output of the free running chopper is fed into a transformer which generates the output voltage based on the magnitude of the source voltage. A relay selects the secondaries of a center-tapped transformer which yields either 120V or 240V AC output levels. The output is rectified to form a square wave with a duty cycle of 90-92%. This is done to minimize the ripple and stress on components. A snubber circuit is in place to bleed current from the parasitic capacitance of the inductor and voltage spikes which occur during the off period of the duty cycle.

Synchronization of the chopper circuitry is handled through the PIC17C43. In the event of a loss of the synchronization signal, the chopper has an internal synchronization source.

Inverter and Output Filtering

The input to the inverter is the free running chopper rectified square wave. After appropriate DC Bus filtering, this waveform is fed into the H-bridge circuit (Figure 2). The H-Bridge is under the control of a PIC17C43 running at 25MHz.

The output of the H-Bridge (differentially) consists of a waveform of rectangular pulses with a constant frequency of 25kHz and a duty cycle that varies to correspond with the absolute value of the desired output sine wave. Output filtering produces the smooth sine wave.

There are snubber circuits on Q9 and Q10 of the H-Bridge which discharge spikes back onto the DC bus to minimize component stress.

The inductors L1 and L2 suppress ripple and additional inductors, capacitors and discretes provide further filtering of the output voltage.

Hardware Protection and IGBT Drivers

The PIC17C43 controls the inverter through the hardware protection circuitry and the drivers for the H-Bridge. Insulated Gate Bipolar Transistors (IGBTs) are used for the H-Bridge rather than MOSFETs due to their lower ON resistance. Although IGBTs have a slower turn on time than MOSFETs, the relatively low frequency of operation (PWM frequency = 25kHz) makes this property irrelevant.

Inverter control signals connect the PIC17C43 and the inverter through the hardware protection circuit and the IGBT drivers. These control signals are: ENABLE, FAULT, POS_NEG and PWM. See *System Overview - Inverter Operation* for a detailed discussion of how PIC17C43 signals control the H-Bridge inverter.

ENABLE will enable or disable all drive capability to the H-bridge. This is a local enable.

A FAULT will override the ENABLE, but can be reset in the software so that a hardware retry may be attempted.

A FAULT can also be generated by the H-bridge circuitry directly in order to shut done the IGBTs as quickly as possible (Hardware, or HW, FAULT). In the event of a catastrophic failure, H-bridge hardware can respond faster than the PIC17C43 software. This will prevent damage to the IGBTs.

The POS_NEG signal controls the H-Bridge modulation for either positive or negative wave generation.

The modulation scheme (using PWM) is inherent in the hardware protection circuitry. The hardware protection also allows for a dead time on the IGBTs during state transitions.

Output Monitoring Using A/D Converter

Feedback of the output AC sine wave is accomplished through the use of an external 8-bit A/D converter. An 8-bit A/D is considered adequate based on the speed of operation of the PIC17C43 and the resolution needed for 120V.

Both the output current and output voltage are monitored through the A/D converter. The voltage is sensed at the output stage and is fed to the A/D through an op amp circuit. The voltage is attenuated to the A/D input range. An op amp is used so that any DC offset components remain with the signal and can be measured. The current is monitored through a current transformer.

The current and voltage inputs are used to correct for any errors in the magnitude of the output wave. The output voltage is sampled 32 times per half-wave which results in an output wave with 1.5% distortion (resistive load with feedback) while running the PIC17C43 at 25 MHz.

Power factor correction also makes use of the feedback signals, as well as zero crossing. Information about the output wave is compared with zero crossing information about the input wave to provide input/output synchronization. The zero crossing detect signal comes directly from the input wave and is used to indicate if a zero crossing point has been detected. The PIC17C43 then measures from point-to-point on the zero crossing to calculate the frequency of the input wave. This data is used to generate a sine wave of the same frequency through internal look-up tables.

Note:	Power factor correction has not been implemented in PICREF1.

SOFTWARE OVERVIEW

The PIC17C43 embedded software controls the operation of the AC sine wave generation. It is imperative that the loop response be fast enough to minimize distortion on the output wave. Therefore, the throughput of the microcontroller is a critical parameter.

The architecture of the PIC17C43 provides enough throughput to execute the control algorithm with a minimum of distortion. The architecture is efficient enough to support the device running at 33 MHz (121 ns instruction cycle), so can easily support 25 MHz (160 ns instruction cycle) to meet the distortion requirement. The system described in this paper has a measured total distortion of 3% (resistive load) without feedback and 1.5% THD with feedback. The load regulation with feedback was measured to be 0.8%.

The flow diagram for the software is shown in Figure 7. The main software function looks for the zero crossing point and calculates the input frequency. Based on the calculation, the appropriate look-up table is indexed. The SW checks for violation of maximum conditions and sets the appropriate flags. The loop continues indefinitely based on the zero crossing detect.

Information on how the look-up table is generated is provided in the first subsection.

The interrupt is set up to occur periodically based on the output frequency of the wave. The interrupt period is initialized so that 32 interrupts occur within the half-wave period. During the interrupt, there must be sufficient margin to perform two A/D conversions (current and voltage), calculate offsets and errors, and adjust the output duty cycle. The interrupt flow diagram is shown in Figure 8.

Adjusting the AC output waveform requires adjusting the PWM that controls the inverter circuitry (H-Bridge). To do this, compensator coefficients need to be determined. That is, in pseudocode:

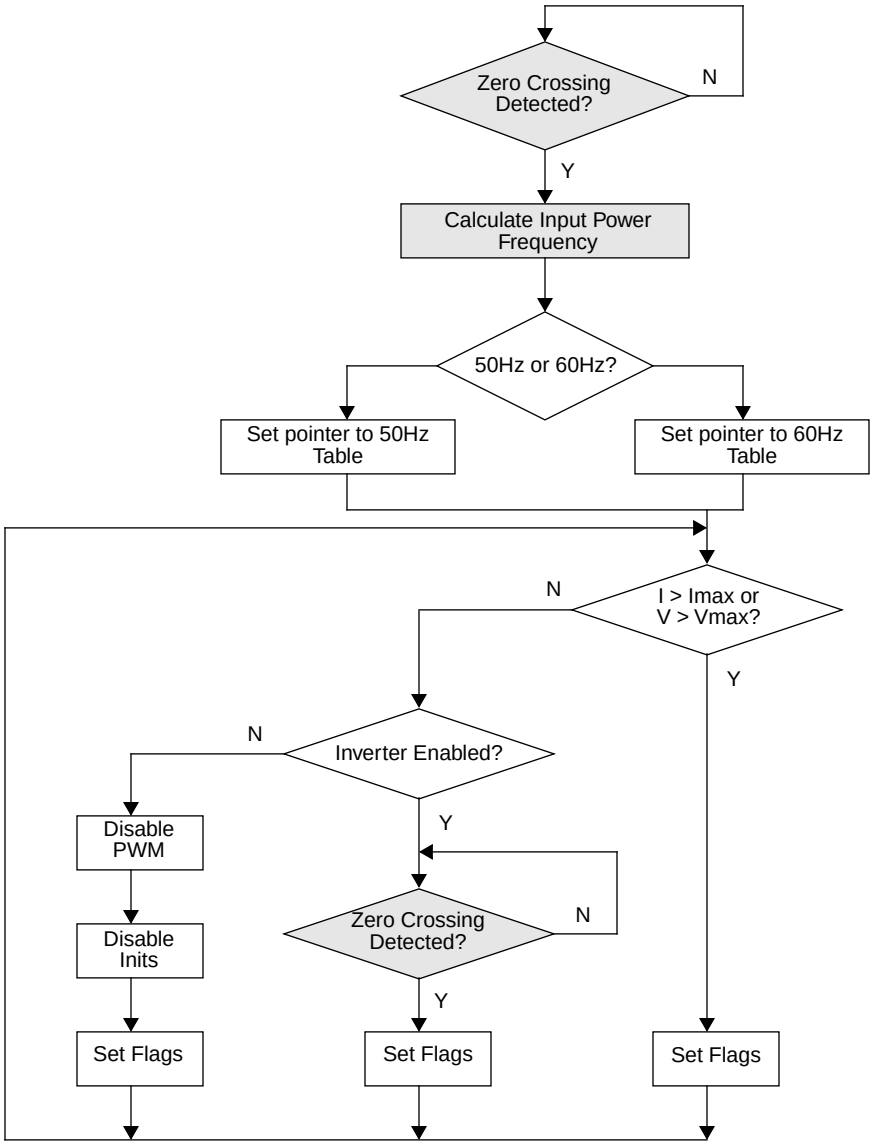
```
X = (Output_V) - Vref;
Y = c * Yold + d(X + Xold);
Yold = Y;
Xold = X;
```

Where `Y = output; X = error.`

How to calculate the coefficients c and d for a single-pole compensator is shown in the second subsection.

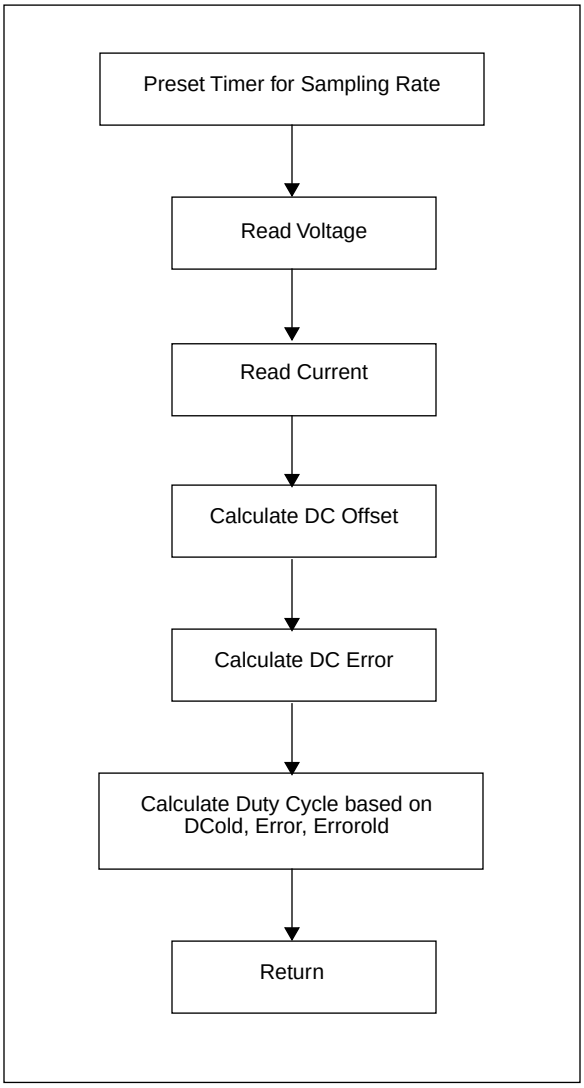
A listing of all UPS PIC17C43 software is shown in Appendix C.

FIGURE 7: MAIN PROGRAM FLOW



Shaded objects indicate provisional sections.
Power factor correction not implemented.

FIGURE 8: INTERRUPT HANDLER FLOW



Look-Up Table

The sinusoidal reference table for the DSP-based inverter is generated as follows:

1. Choose Vp such that this number corresponds with the desired output voltage of the inverter. Example: If the desired output voltage is 120V and the A/D converter used to sample the output voltage has a gain of 1.5 counts per output volt, then:

   $$Vp = 1.5(120\sqrt{2})$$

   and Vp would be equal to 254.6, or 255 rounded to the nearest integer.

   The external circuitry interfacing the A/D converter to the output of the inverter should scale the input voltage to the A/D such that the peak of the desired output voltage should correspond to almost a full count on the A/D.

2. The table is generated from the following equation with k = 0.... N/2 - 1 and N = the number of samples per cycle.

   $$Vref = Vp\sin\frac{2\pi k}{N}$$

   Example: For the Vp of the previous example and N = 64 samples per cycle, this yields the following table entries. Note that only 32 entries are generated as the negative-going halfwave may be generated from the negative of the first 32.

   Vref = 0, 25, 50, 74, 98, 120, 142, 162, 180, 197, 212, 225, 235, 244, 250, 254, 255, 254, 250, 244, 235, 225, 212, 197, 180, 162, 142, 120, 98, 74, 50, 25.

Calculating the Compensator Coefficients

A convenient way of determining the coefficients for an IIR (Infinite Impulse Response) compensator from an analog transfer function in the Laplace (s) domain is the Bilinear z-transform. The following example illustrates the technique for a compensator with a single pole.

EXAMPLE 1: SINGLE-POLE COMPENSATOR

An inverter is designed that requires a compensator of the form:

$$H(s) = \frac{a}{s+b} \quad (1)$$

The first step is to normalize H(s) and make note of the cutoff frequency (cutoff frequency = b):

$$H'(s) = \frac{(a/b)b}{s+1} \quad (2)$$

Choose a sampling frequency at least 32 times the desired output frequency (i.e., 1.92kHz for a 60 Hz inverter). If the desired gain crossover frequency of the loop response is more than 1/4 of the chosen sampling rate, a higher rate equal to at least 4 times the gain crossover frequency should be used.

Make the following substitution in (1):

$$s = \alpha\frac{z-1}{z+1} \quad (3)$$

Where α = cot(b * T/2).

Thus,

$$H(z) = \frac{a(z+1)}{\alpha b(z(\alpha+1)-(\alpha-1))} \quad (4)$$

The last step is to determine the difference equation that will yield the transfer function of (4).

$$y(z) = H(z) \bullet x(z)$$

$$y(z)[\alpha b(z(\alpha+1)-(\alpha-1))] = a(z+1)x(z) \quad (5)$$

Multiplying both sides by (1/z) and using the fact that;

$$Z[y[k-n]] = z^{(-n)}Z[y[k]] \quad (6)$$

yields the desired difference equation.

$$y[k] = \frac{\alpha-1}{\alpha+1}y[k-1] + \frac{a}{2(\alpha+1)(b)}(x[k]+x[k-1] \quad (7)$$

DC Offset Correction

DC Offset is corrected for by taking the DC offset from a single cycle. This offset is integrated over time and used to correct the output wave. The DC offset is added to the sine wave to determine the point-to-point magnitude. This is then compared to the reference sine wave to determine DC offset correction.

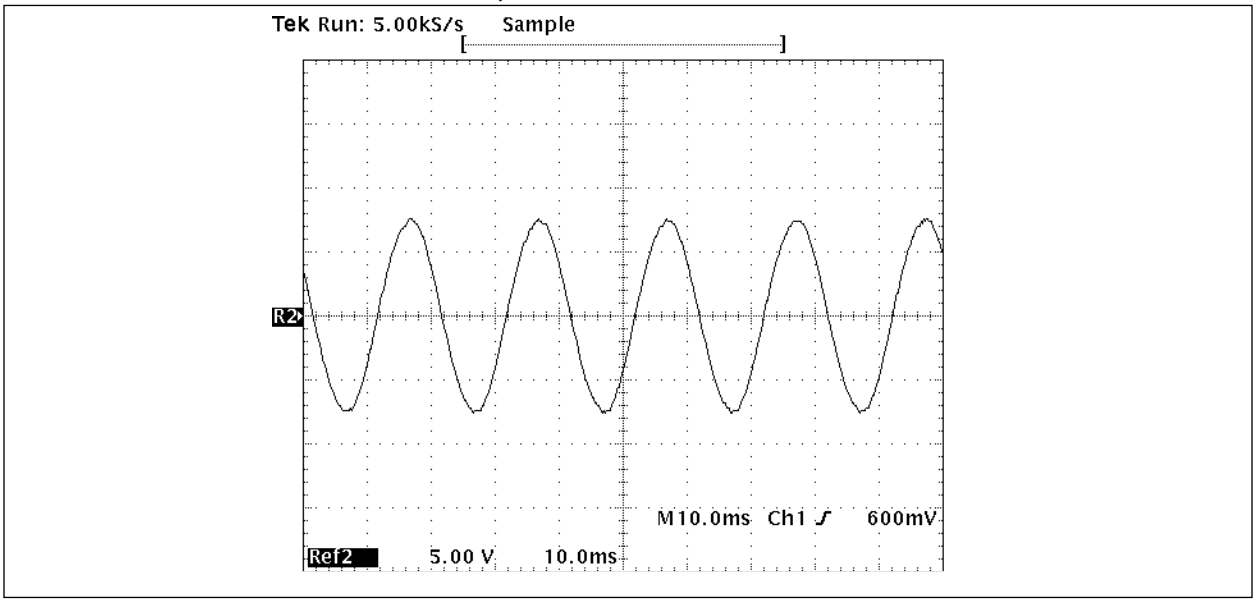
TEST RESULTS

No Load Conditions

Figure 9 is an example output waveform under no-load, no feedback conditions.

The example output waveform is a stepped-down versions of the actual output waveform, available for oscilloscope display by placing a probe on the UPS “Load Monitor” BNC connector.

FIGURE 9: AC OUTPUT - NO LOAD, NO FEEDBACK



Load Conditions

Figure 10 is an example output waveform under load, no feedback. The load used was resistive, drawing 8.6 Amps.

This example output waveform is a stepped-down version of the actual output waveform, available for oscilloscope display by placing a probe on the UPS “Load Monitor” BNC connector.

Figure 11 is an example output waveform under load, with feedback. The load used was resistive and inductive, drawing 4 Amps.

This example output waveform is the actual UPS output waveform.

FIGURE 10: AC OUTPUT - RESISTIVE LOAD, NO FEEDBACK

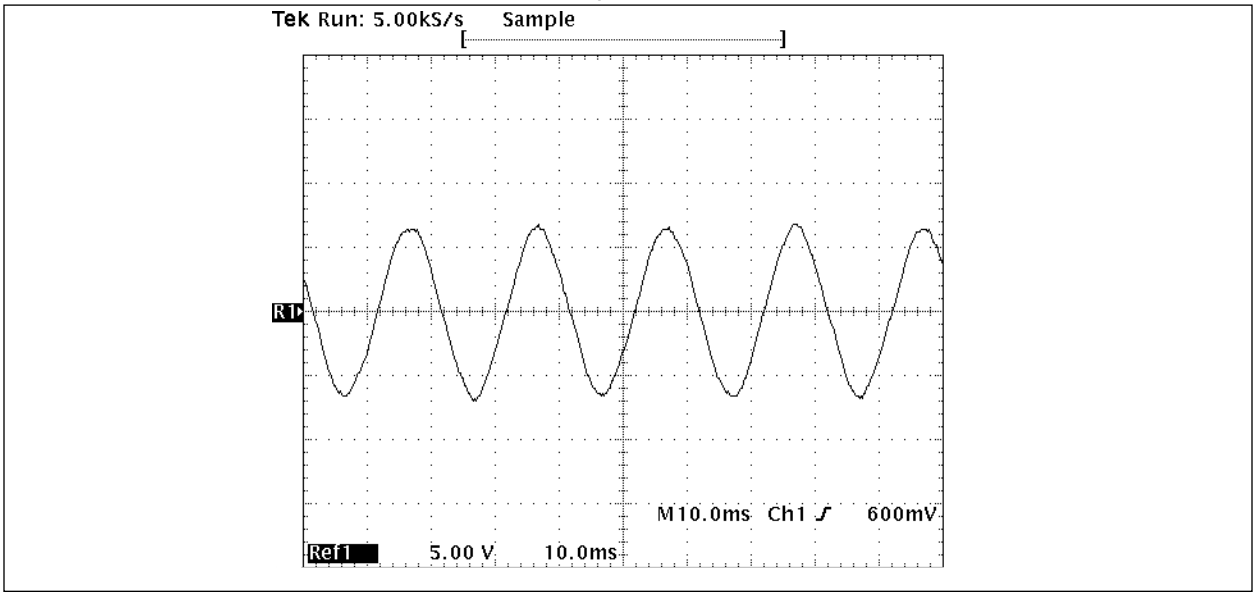
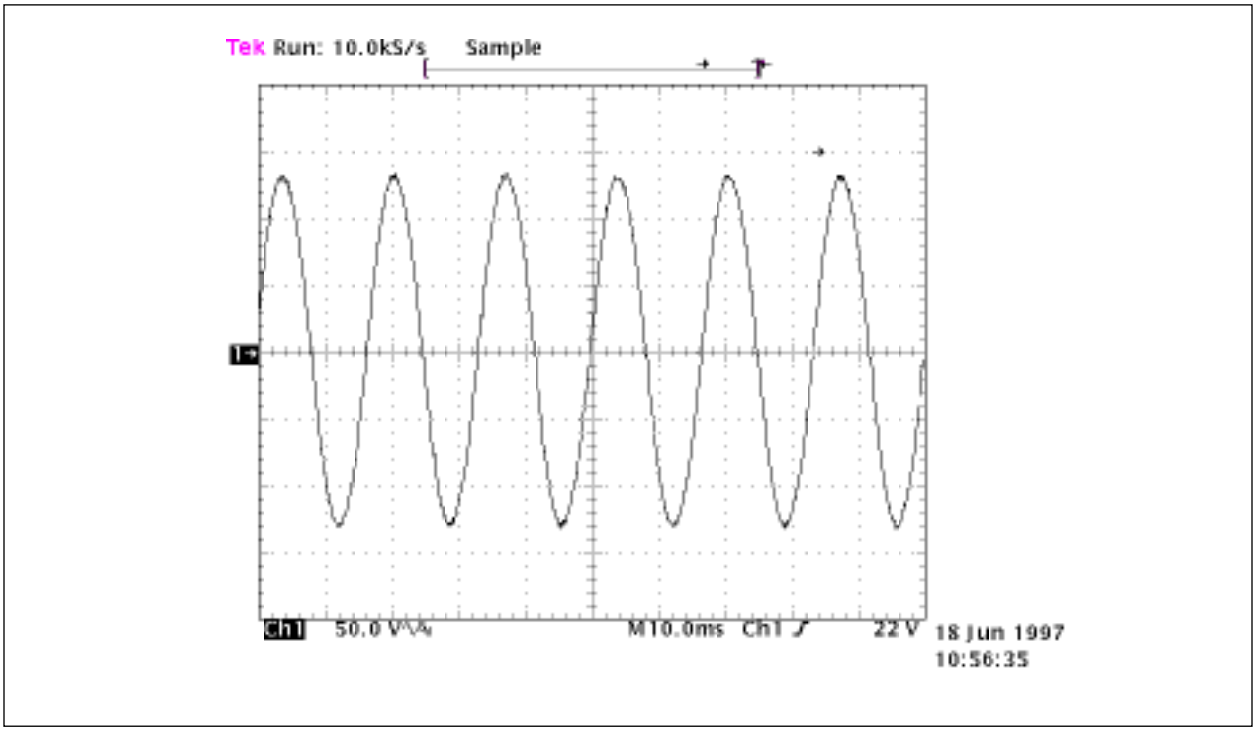


FIGURE 11: AC OUTPUT - RESISTIVE AND INDUCTIVE LOAD WITH FEEDBACK



DESIGN BACKGROUND

An example of how to implement a UPS system using a microcontroller has been described in the previous sections. However, if a customer wishes to change part or all of this reference design, then understanding the reasons why the design was developed as it was must be understood.

When designing a UPS system, there are three items that must be considered: cost vs. performance, output waveform and topology.

Cost vs. Performance

A UPS system has to be reliable. Money saved on features or performance can be overshadowed by the cost associated with data loss or component failure. So it is important to develop a cost effective solution which satisfies both end user price sensitivity and design robustness.

By incorporating a PIC17C43 microcontroller into the UPS design, the number of necessary components is reduced, thus reducing cost. Also, PIC17C43 peripherals and speed enhance the performance of the UPS system. Software control of the PIC17C43, and thus the UPS, allows for ease of modification and addition of special features. So in terms of cost vs. performance, the PIC17C43 offers a win-win solution.

Other components of this reference design were chosen considering cost and performance. However, there are other design options which are discussed in the section *Design Modifications*.

Output Waveform

Some UPS designs use a square wave output instead of a sine wave. This makes the system cheaper to produce. But is this type of waveform really acceptable?

Electrical equipment uses power delivered in the form of a sine wave from local utility companies. When considering alternative waveforms, how differing loads rely on different parts of the standard power company waveform must be examined.

For instance, most appliances are always on, thus the power used by the appliance is the RMS value of the sine wave, which is approximately 120 volts. However, equipment such as computers use peak voltage values, which are approximately 170 volts.

When a square wave output is used to supply power to computer equipment, the RMS and peak values are equivalent, thus stressing some loads and under-supplying others. So the best output to provide electrical equipment is the output that they are designed to operate with - a sine wave.

The speed of the PIC17C43 allows this reference design to produce a sinusoidal output AC waveform. This causes less stress on all electrical equipment. Actual output waveform graphics are provided in the section *Test Results*.

Topology

To an end user, the function of a UPS system is much more important than form. Despite the many variations of UPS systems on the market, they can be boiled down into two major topologies: Off-line and On-line UPS.

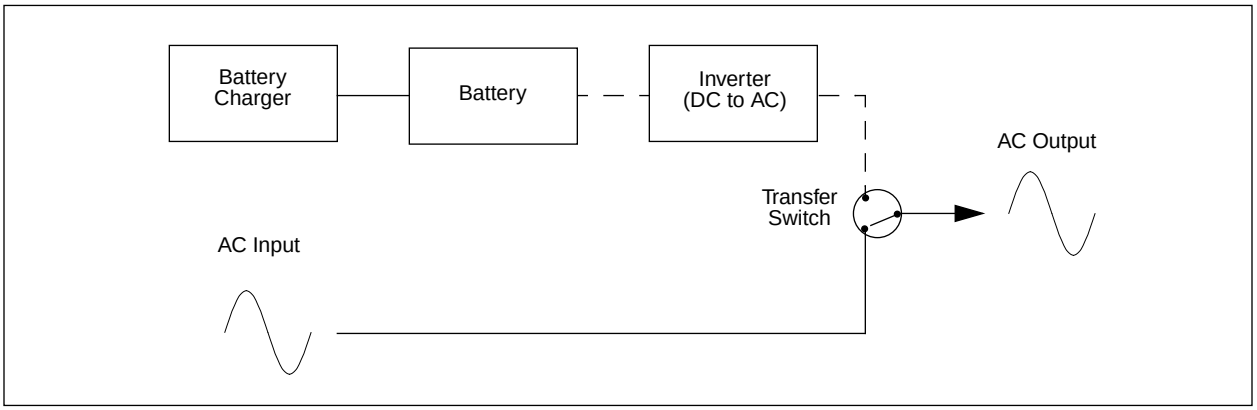
Off-Line UPS

The first topology is known as off-line or standby, meaning that the inverter is normally off-line. A block diagram of an off-line UPS is shown in Figure 12. (The solid line represents the primary power path and the dashed line represents the secondary or back-up power path.)

In normal operation, the output power comes from the input power source. This implies that there is a transfer time in switching the inverter on-line during a power interruption. If this transfer time is too great, there will be a less than smooth transition for the load on the UPS. This could lead to the same problems that the UPS was designed to avoid.

The advantage of this topology lies in the fact that the stress on the inverter is decreased due to the inverter being turned off during normal operation. However, since the inverter only runs during power interruptions, this feature lends itself to latent failures when back-up power is needed the most.

FIGURE 12: OFF-LINE UPS



On-Line UPS

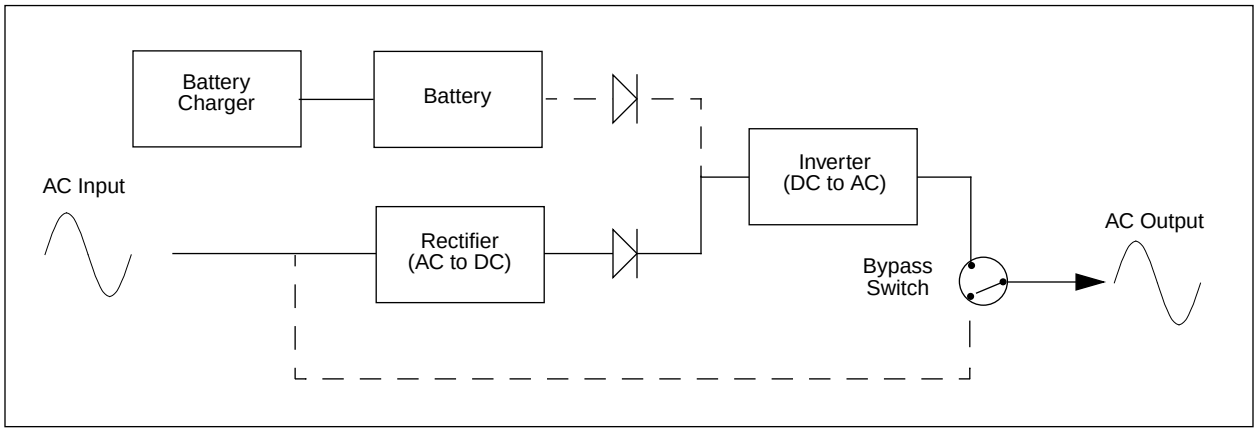
The other major topology is the on-line or true UPS. As the name implies, the inverter is always on-line. A block diagram of the on-line UPS is shown in Figure 13.

At start-up the UPS is in bypass mode until the inverter is running and synchronized with the input power source. Control is then transferred to the inverter. The inverter remains on-line during normal operation and during power failure operation until the battery is exhausted. During an inverter failure, the power is switched back to primary power through the bypass switch. This allows for the failed condition to be corrected while AC input power is still good.

The one drawback to the on-line topology is that the inverter is always on-line. This would imply that the "life" of this topology would be shorter than an off-line UPS. However, the life of a UPS in practice has more to do with the robustness of the design than the topology used.

The topology used for this reference design is the true (on-line) UPS.

FIGURE 13: ON-LINE UPS



DESIGN MODIFICATIONS

This reference design is for guidance only, and it is anticipated that customers will modify parts of it. With this in mind, this section suggests modifications that the customer may wish to make to the design.

- The PIC16/17 family of microcontrollers offers a wide variety of options for a UPS design from the PIC16C72 to the PIC17C756. The PIC16C72, PIC16C73A, PIC16C74A, PIC17C43, and PIC17C756 all have the processing throughput to generate the sine wave described in this documentation.

  For this design (PIC17C43), the frame rate for 64 point sampling of a 60Hz sinewave is 260 usec. The feedback code is approximately 200 instructions, which yields a frame usage of 30 usec of the 260 usec. This leaves a margin of 230 usec for additional housekeeping features (serial communications, battery management, error detection, fault reporting, etc.) that the user may implement.

  In converting the design to a PIC17C756, the user would integrate the A/D functionality. This would add additional time to the frame for the A/D conversion. For instance, if the user wanted to monitor Line Voltage, Line Current, Battery Voltage, Battery Current, this would add approximately 120 usec to the frame. The overall frame usage would increase from 30 usec to 150 usec out of 260 usec, but the external A/D and associated overhead would be eliminated. Additionally, housekeeping features such as battery management, fault detection, and serial communications could be added easily within the remaining frame time.

  In converting the design to a PIC16C72, PIC16C73A, or PIC16C74A, the processor frequency would be decreased and the math required for the sine wave generation would be performed in firmware. This would increase the frame usage by approximately 60-100 usec depending on the desired resolution. Also, the user would integrate the A/D functionality. As described above, Line Voltage, Line Current, Battery Voltage, and Battery Current monitoring would add approximately 120 usec to the frame. The overall frame usage would increase to approximately 210-250 usec out of 260 usec. This would allow minimal housekeeping functionality to be integrated. If serial communications was desired, the PIC16C73A hardware USART would minimize the software overhead required. The PIC16C74A incorporates this feature as well as additional I/O lines if more I/O is needed.

FIGURE 14: PIC16C72 PINOUT

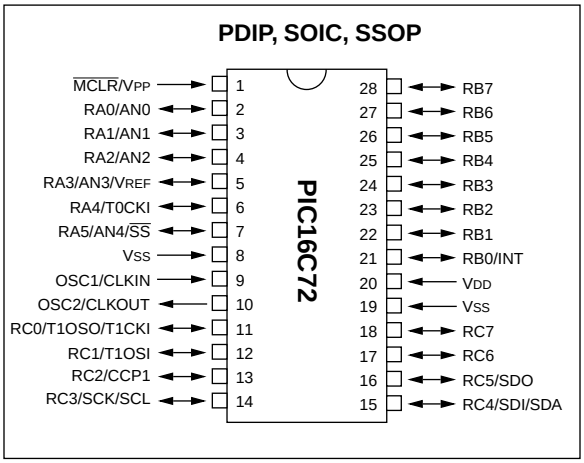


FIGURE 15: PIC16C73A PINOUT

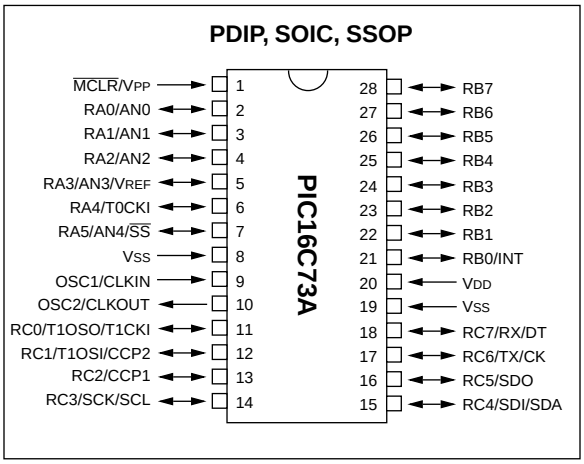


FIGURE 16: PIC16C74A PINOUT

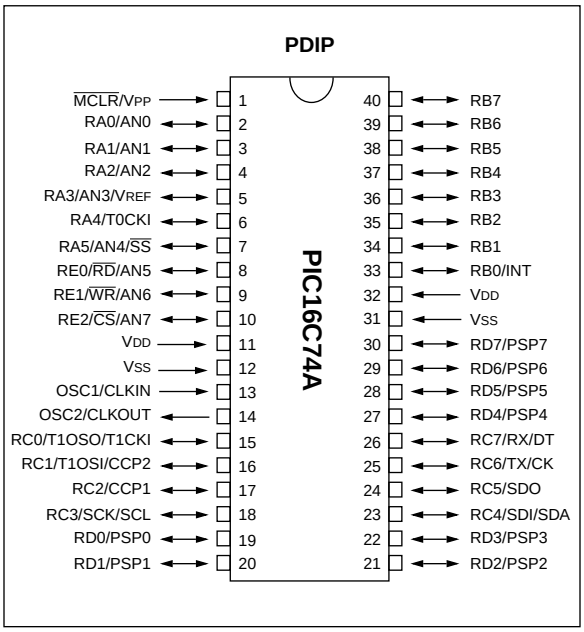
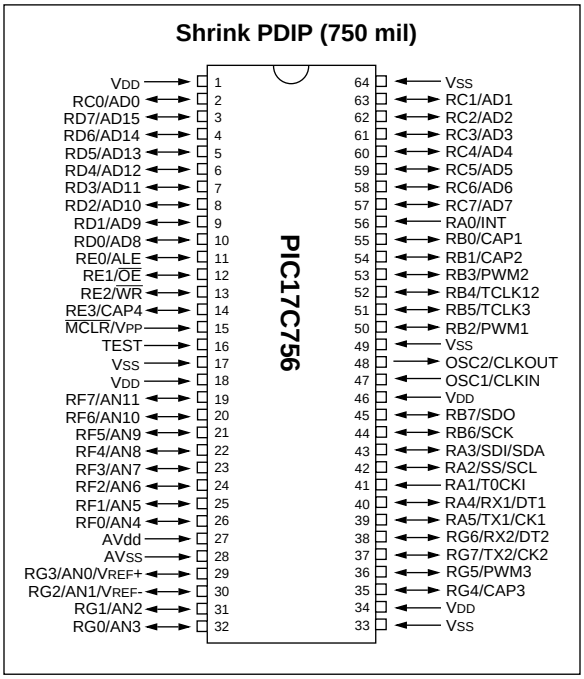


FIGURE 17: PIC17C756 PINOUT



- A different A/D converter for output waveform feedback. An 8-bit A/D is acceptable for 120V, but a 10-bit A/D would yield better resolution for 240V.
- A PAL to replace discrete digital components. Use of external fault detection can also reduce the number of components used.
- MOSFETs are also suitable switching elements for an inverter. They are much faster switches than IGBTs and, in many lower power cases, are less expensive than IGBTs. The faster switching times allow for a higher frequency PWM signal, which would thus require a smaller size/cost output filter to remove the switching frequency from the output. Also, driving MOSFETs may be easier than driving IGBTs.

  The disadvantage of MOSFETs is that their “on” state resistance R_{DS}(on) is large enough to cause dissipation problems for high power inverters and their saturation voltage is less stable over temperature. In addition, as the voltage rating of MOSFETs is increased, their conduction loss increases.

  IGBTs have the benefit that their saturation voltage is a relatively constant 3 volts even when many tens to hundreds of amperes are flowing through the device. This makes for an inverter which has high efficiency at high output currents.

  As for the gate drivers, it is not necessary to use the special IGBT drivers that IGBT manufacturers produce for their product. IGBTs, like MOSFETs, do not draw any continuous gate current, but do have significant amounts for gate capacitance. This requires a circuit that can move the required charge in and out of the gate in short periods of time. Also, the gate drive circuit must have a provision to isolate the high voltage of the IGBT bridge from the logic level voltages on the inverter control PCB. Generally, the hybrid IGBT drivers include some form of out-of-saturation protection circuitry which may or may not be needed based on the application.

APPENDIX A: SYSTEM SPECIFICATIONS

The following is a list of specifications for the UPS unit:

AC Input:	120/240 VAC ± 10%, 50/60 Hz ± 3Hz
UPS Output:	120/240 VAC ± 10%, 50/60 Hz ± 3Hz (User-Selectable), Sinusoidal
Rating:	1400 VA
Input Filtering:	EMI/RFI Filtering
	Metal Oxide Varistor (MOV) for Spike/Surge Protection

APPENDIX B: SCHEMATICS

The UPS schematics shown in this section may be obtained electronically on the Microchip BBS and WWW site (HPGL format; recommend 0.3 pen).

The UPS may be split into 4 main circuits: Input Power Factor Correction, Battery Boost, Free-Running Chopper, and Inverter. The UPS is an on-line device which normally will have the Power Factor Correction circuit feeding the Chopper, which then feeds the Inverter. If the input power should be lost, the Power Factor Correction circuit falls out of the power flow and the Battery Boost circuit automatically provides power to the Chopper.

The Inverter is driven by the Inverter Drive circuitry, which in turn is controlled by the Inverter Control circuitry containing the microcontroller.

UPS circuit board (PCB) power flow is shown in Figure B-1.

B.1 UPS System Overview

In the Battery Boost circuit, the transistor pairs are connected in parallel for the purpose of handling high currents. The current transformer T2 is connected as shown to sense each pair's current with just one transformer, i.e., to prevent it from saturating.

The control for the 120V/240V relay (power switch) was not implemented. Wherever input power monitoring would take place, monitoring for 120 or 240V would also occur and switch the relay. These functions would be placed before the PFC circuit.

B.2 Power Factor Correction

The Power Factor Correction circuit is provisional, so the parts listed are generic parts.

FIGURE B-1: PCB POWER FLOW

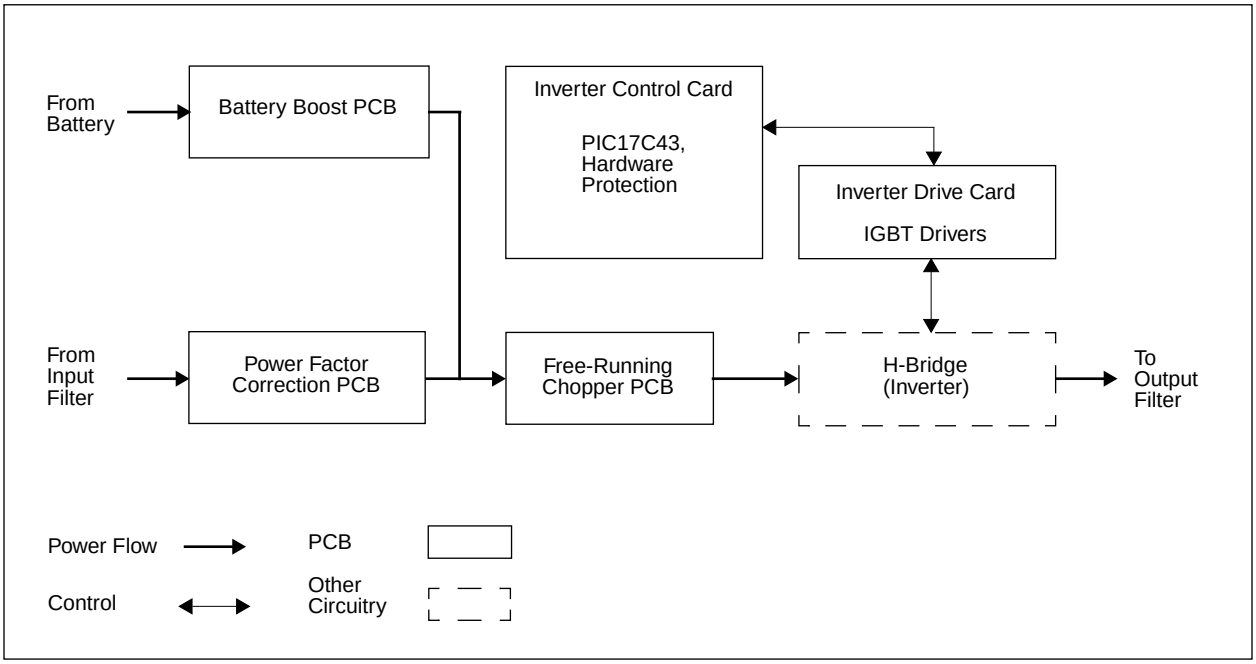


FIGURE B-2: UPS SYSTEM OVERVIEW - PAGE 1 OF 3

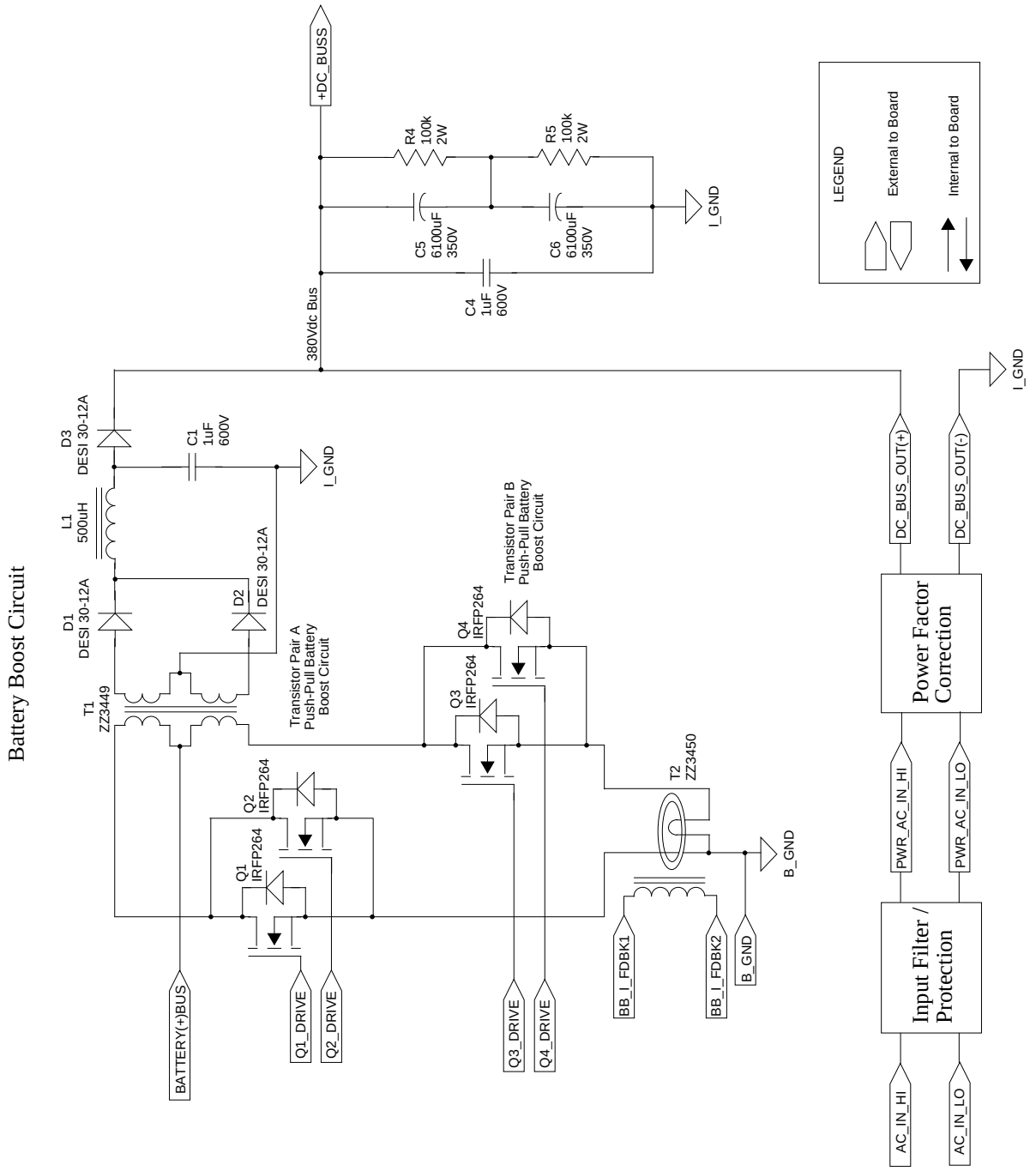


FIGURE B-2: UPS SYSTEM OVERVIEW - PAGE 2 OF 3

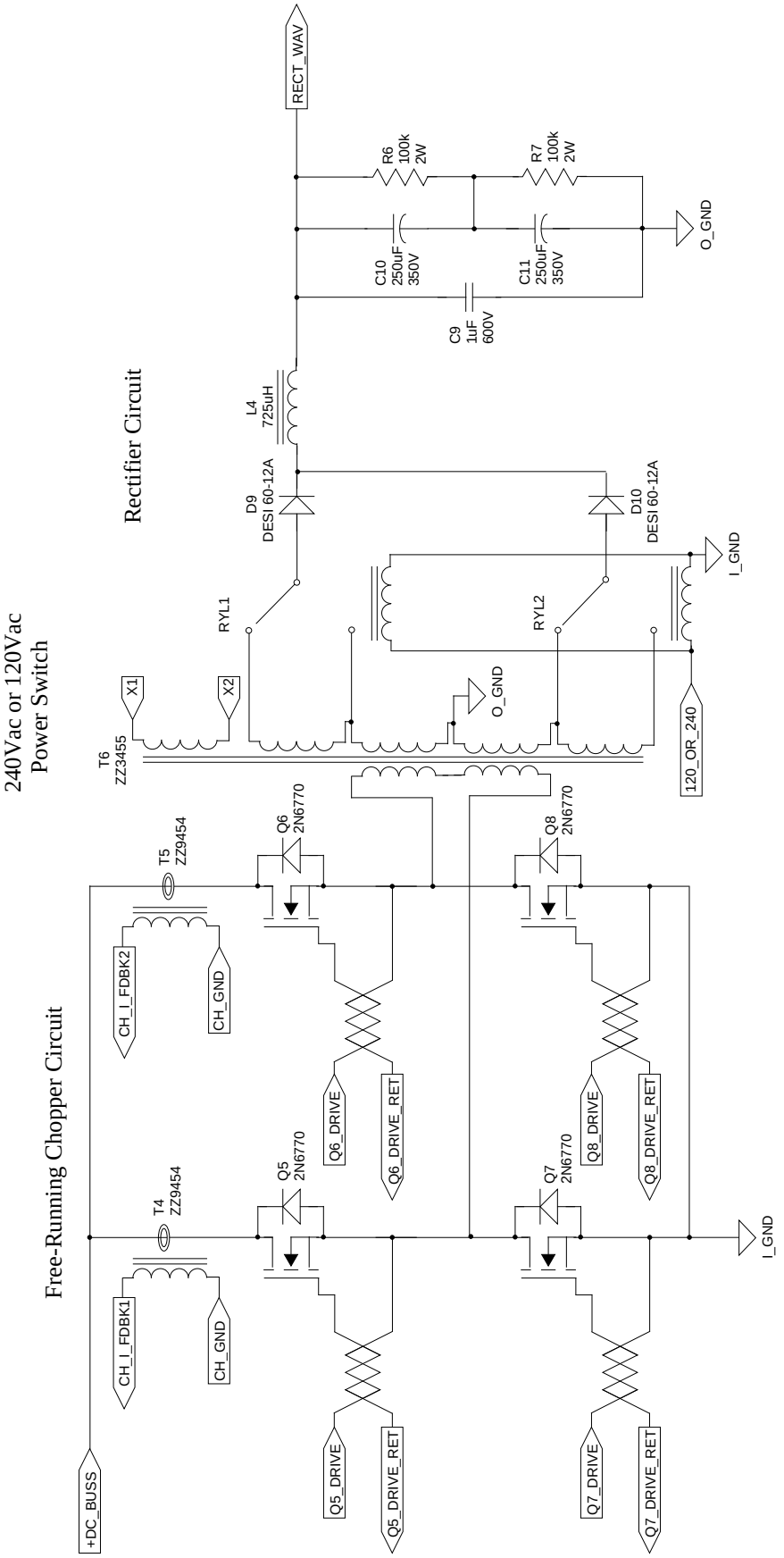


FIGURE B-2: UPS SYSTEM OVERVIEW - PAGE 3 OF 3

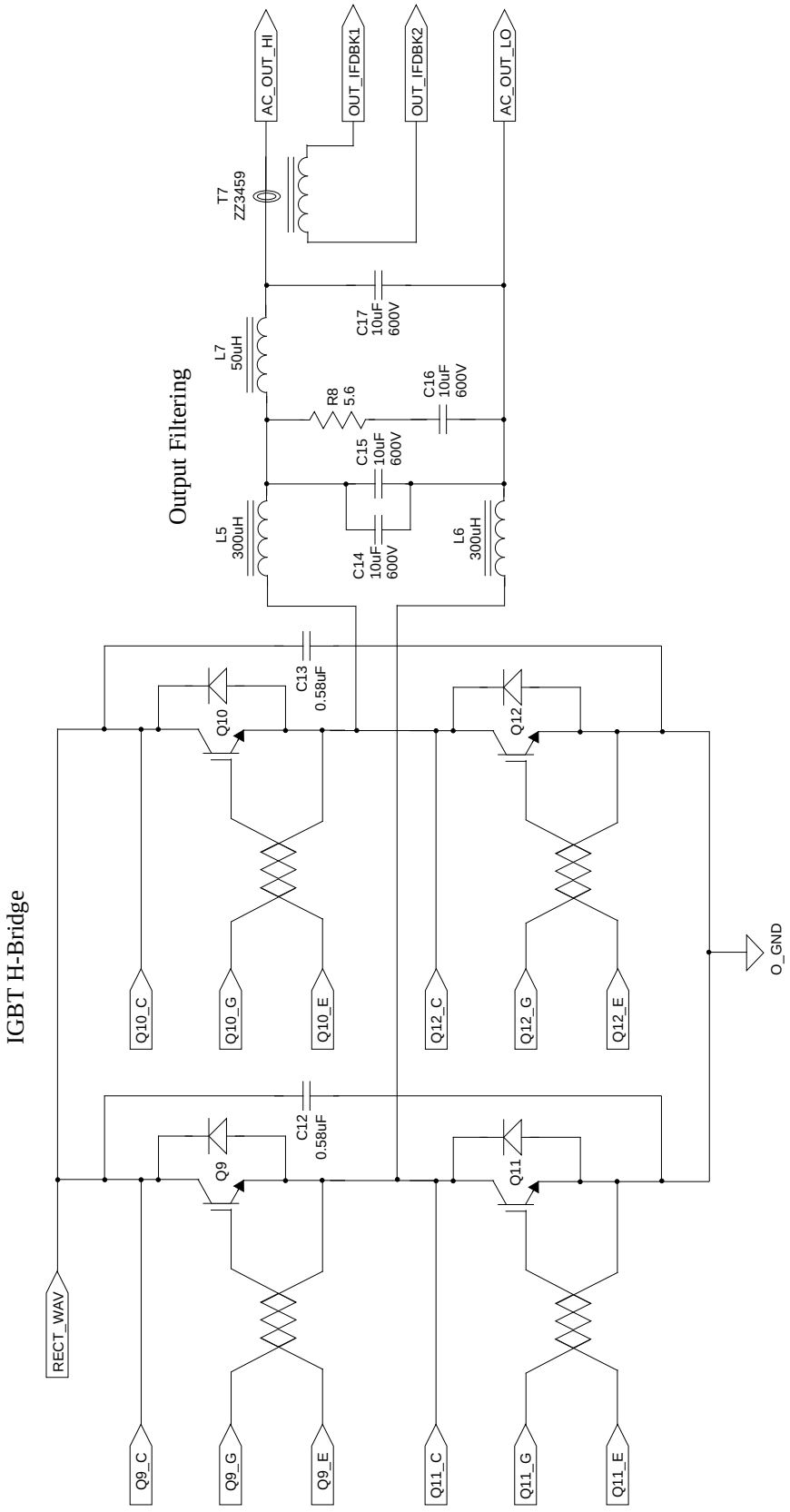


FIGURE B-3: POWER FACTOR CORRECTION (PFC) – PAGE 1 OF 2

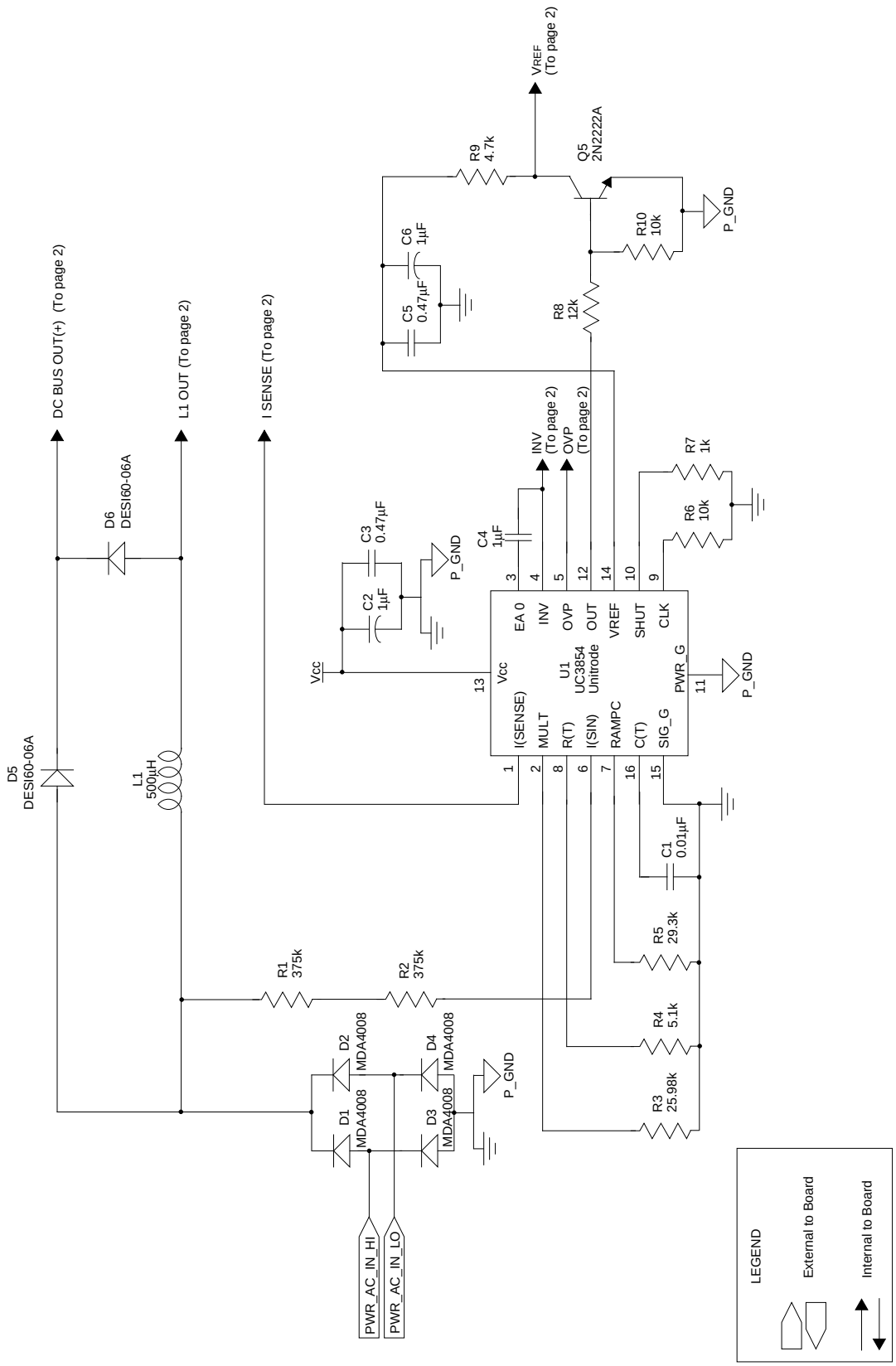


FIGURE B-3: PFC – PAGE 2 OF 2

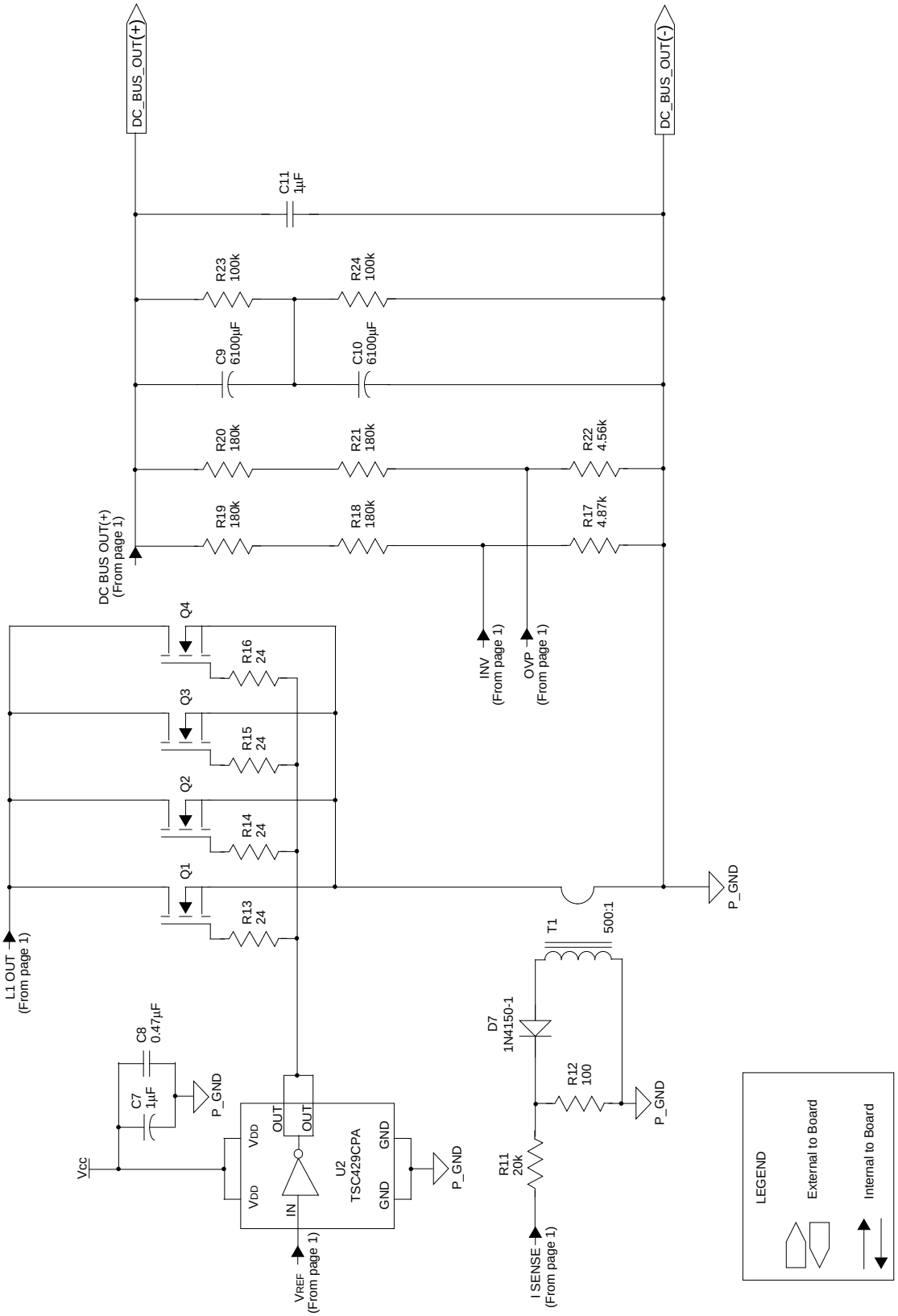


FIGURE B-4: BATTERY BOOST (BB) CONTROL CARD – PAGE 1 OF 3

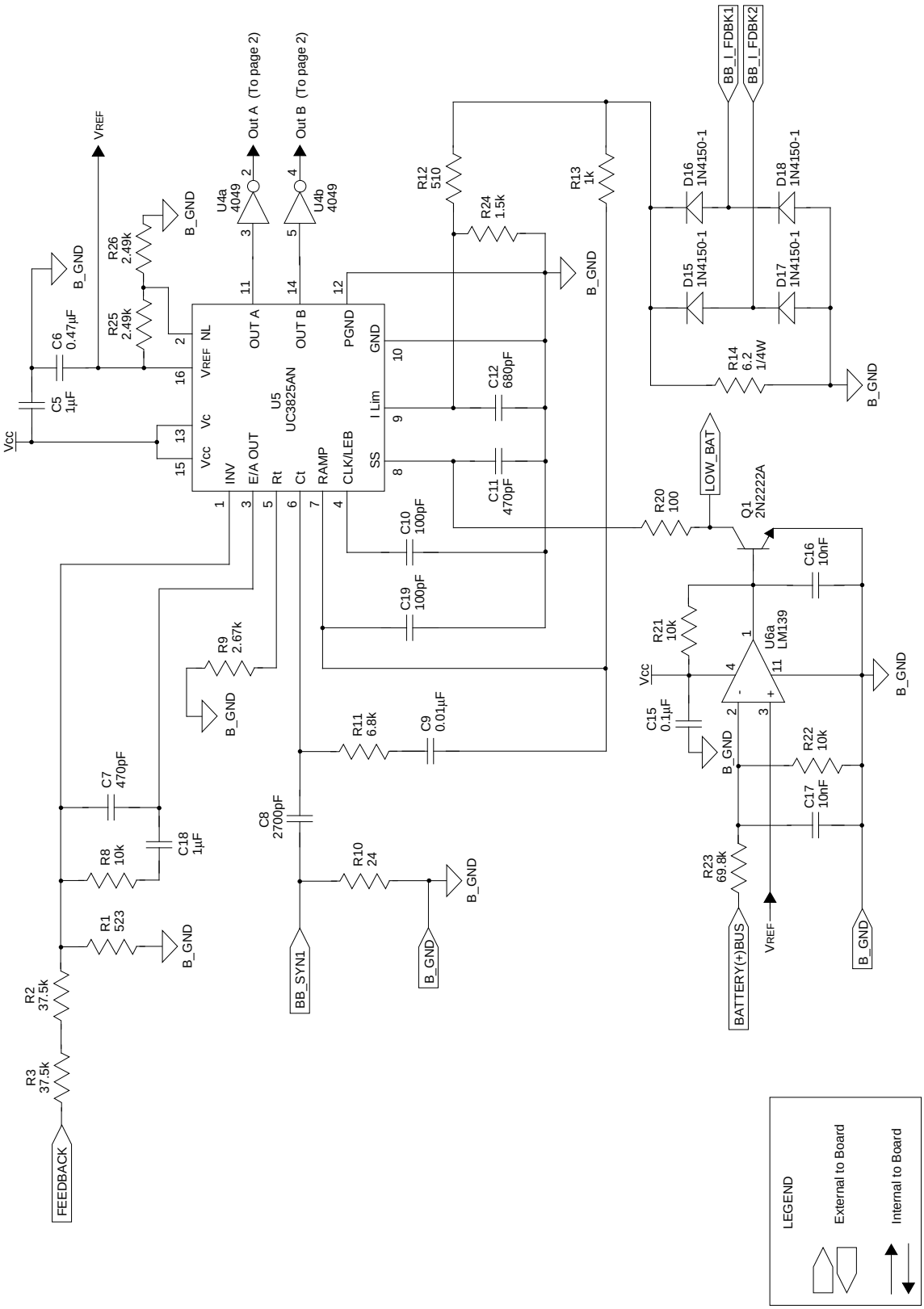


FIGURE B-4: BB – PAGE 2 OF 3

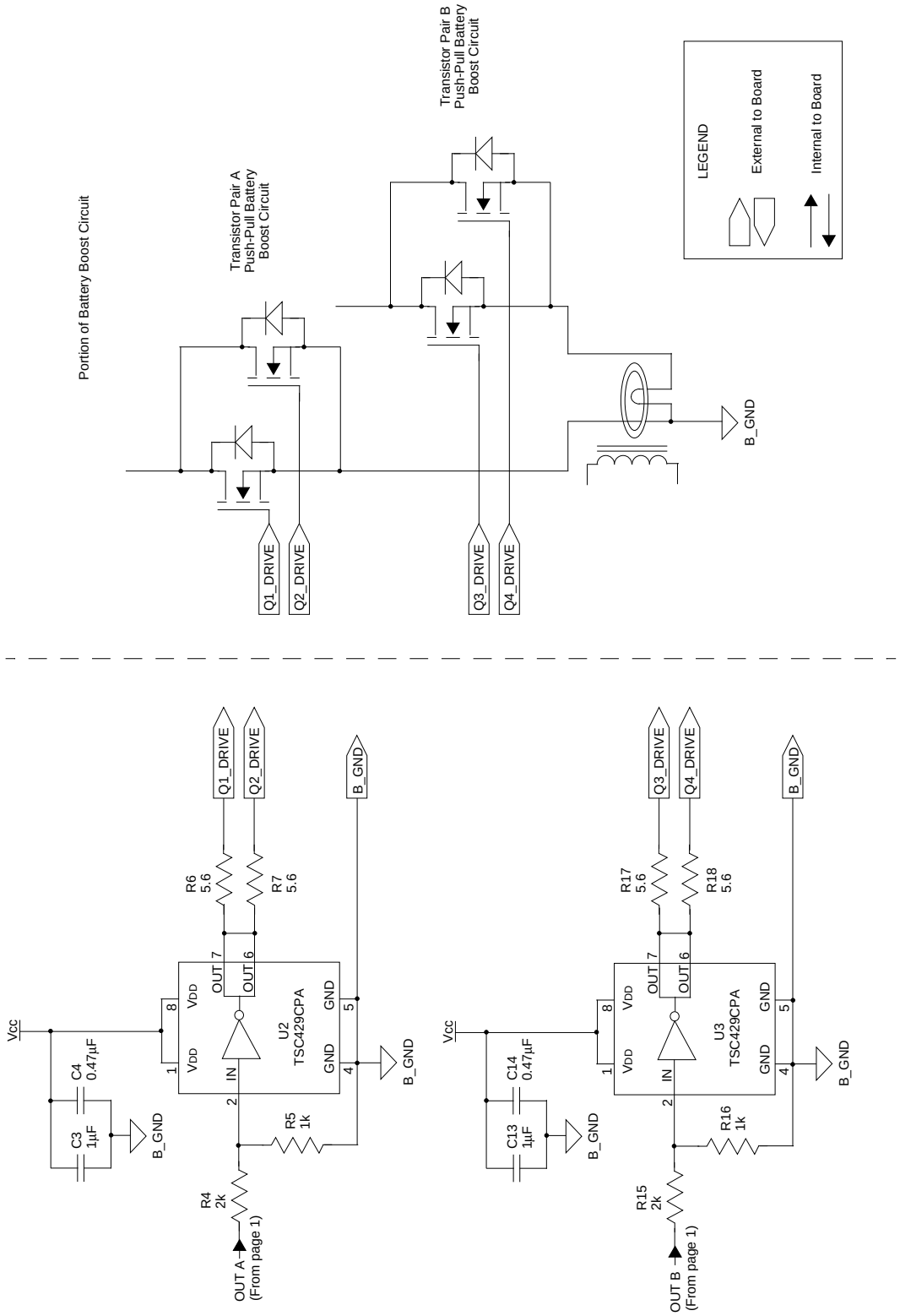


FIGURE B-4: BB – PAGE 3 OF 3

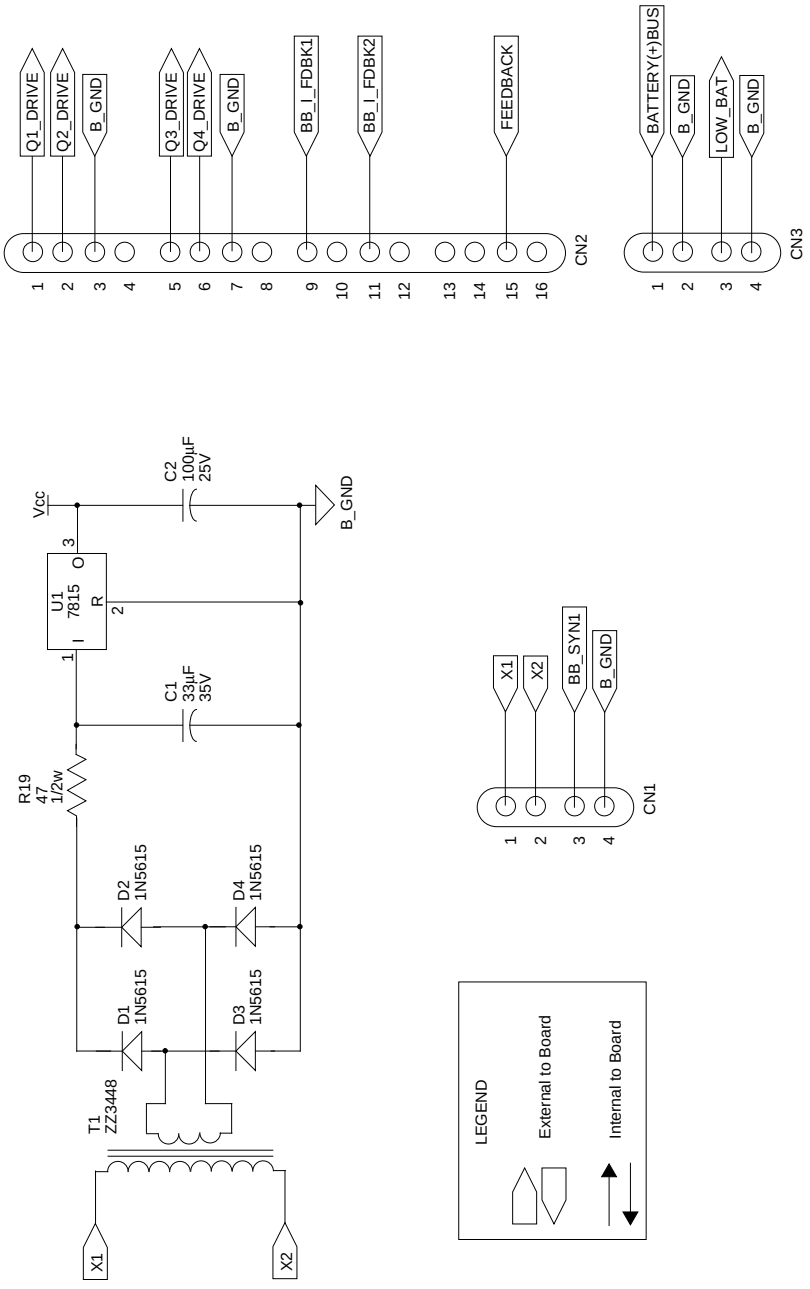


FIGURE B-5: FREE-RUNNING CHOPPER (FRC) CONTROL CARD – PAGE 1 OF 3

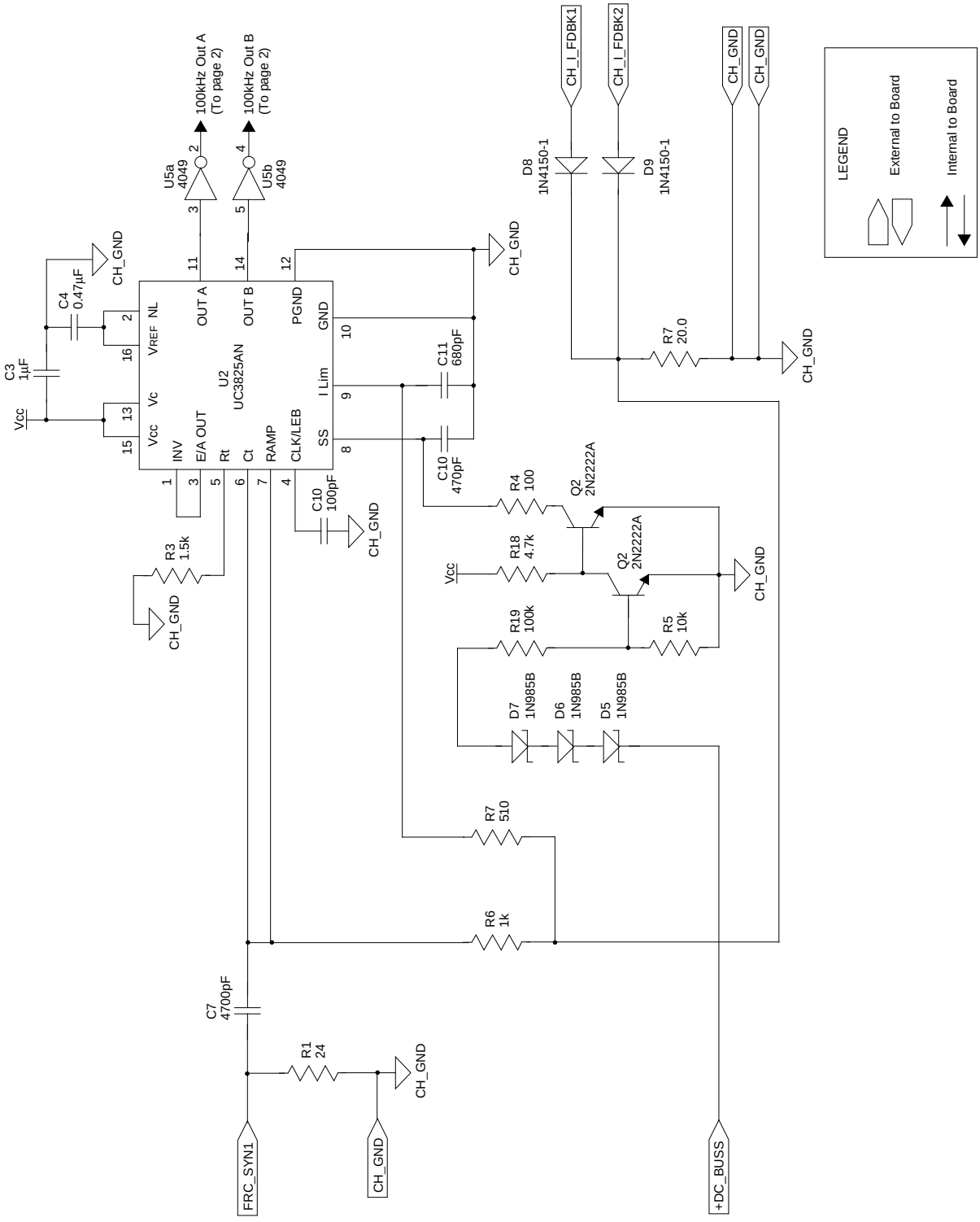


FIGURE B-5: FRC – PAGE 2 OF 3

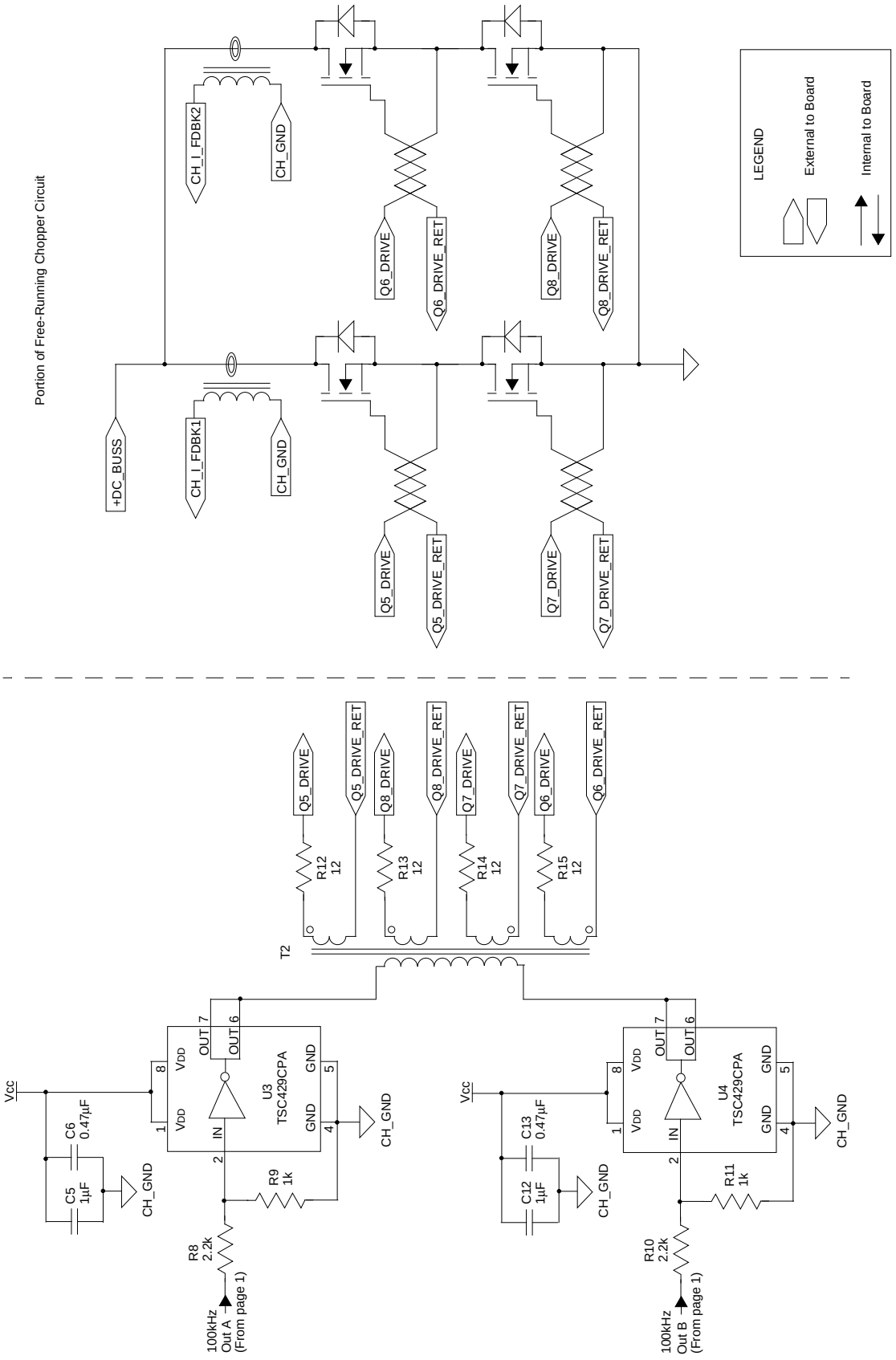


FIGURE B-5: FRC – PAGE 3 OF 3

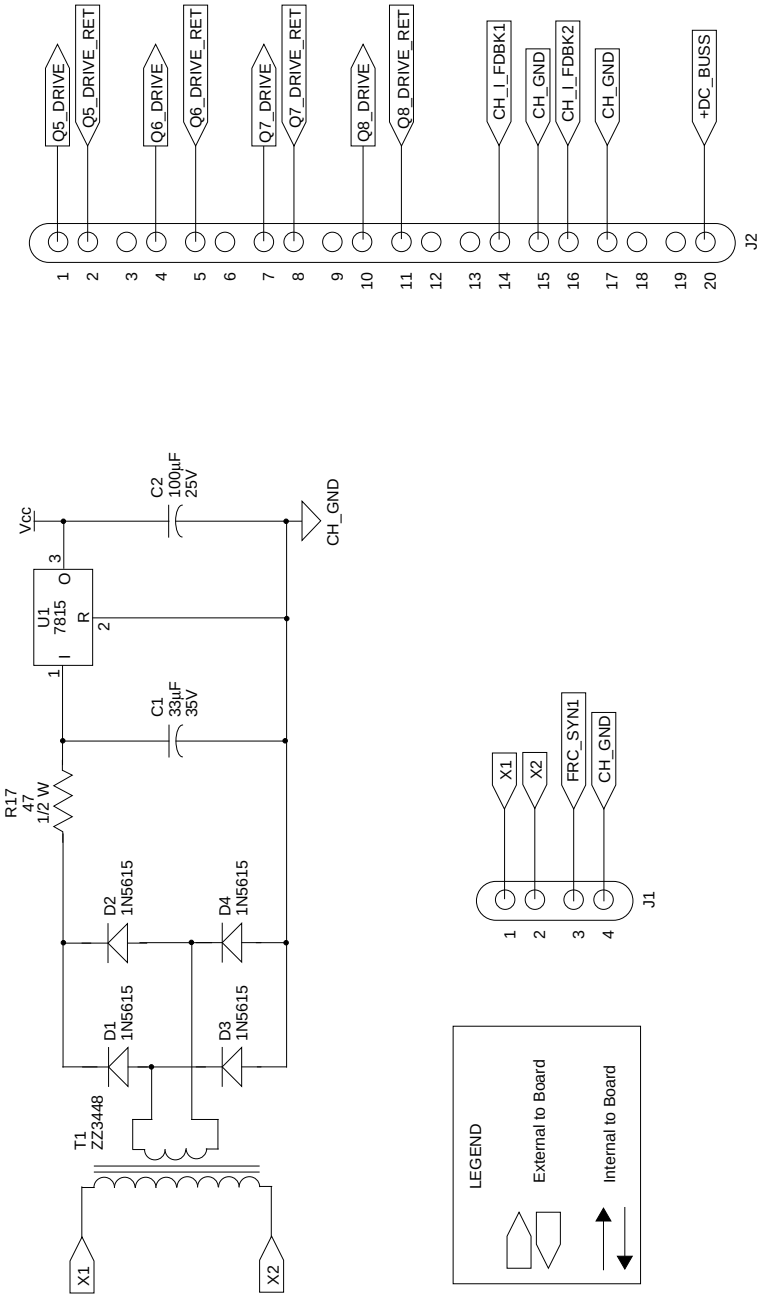


FIGURE B-6: INVERTER CONTROL (INV CRTL) CARD – PAGE 1 OF 4

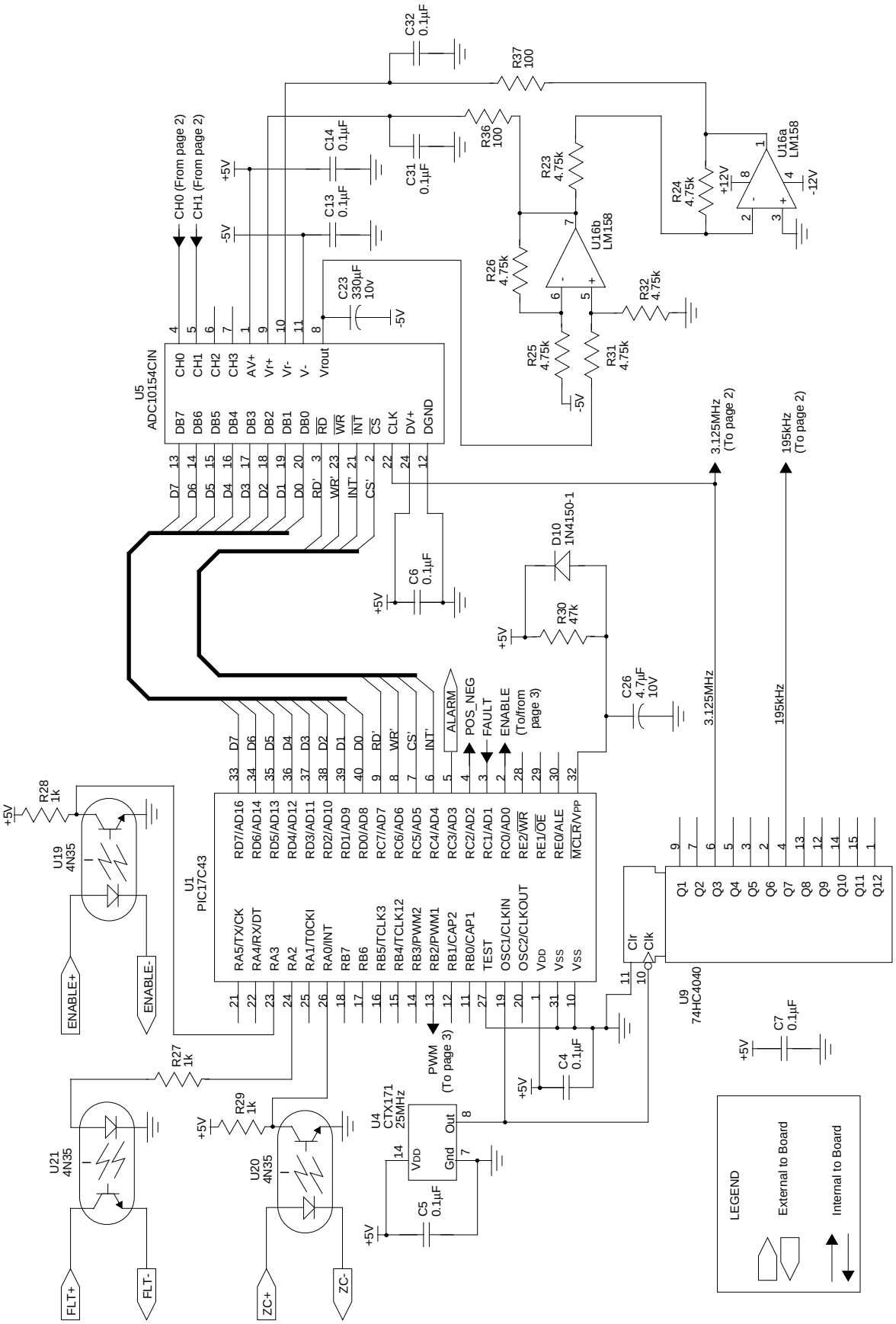


FIGURE B-6: INV CRTL - PAGE 2 OF 4

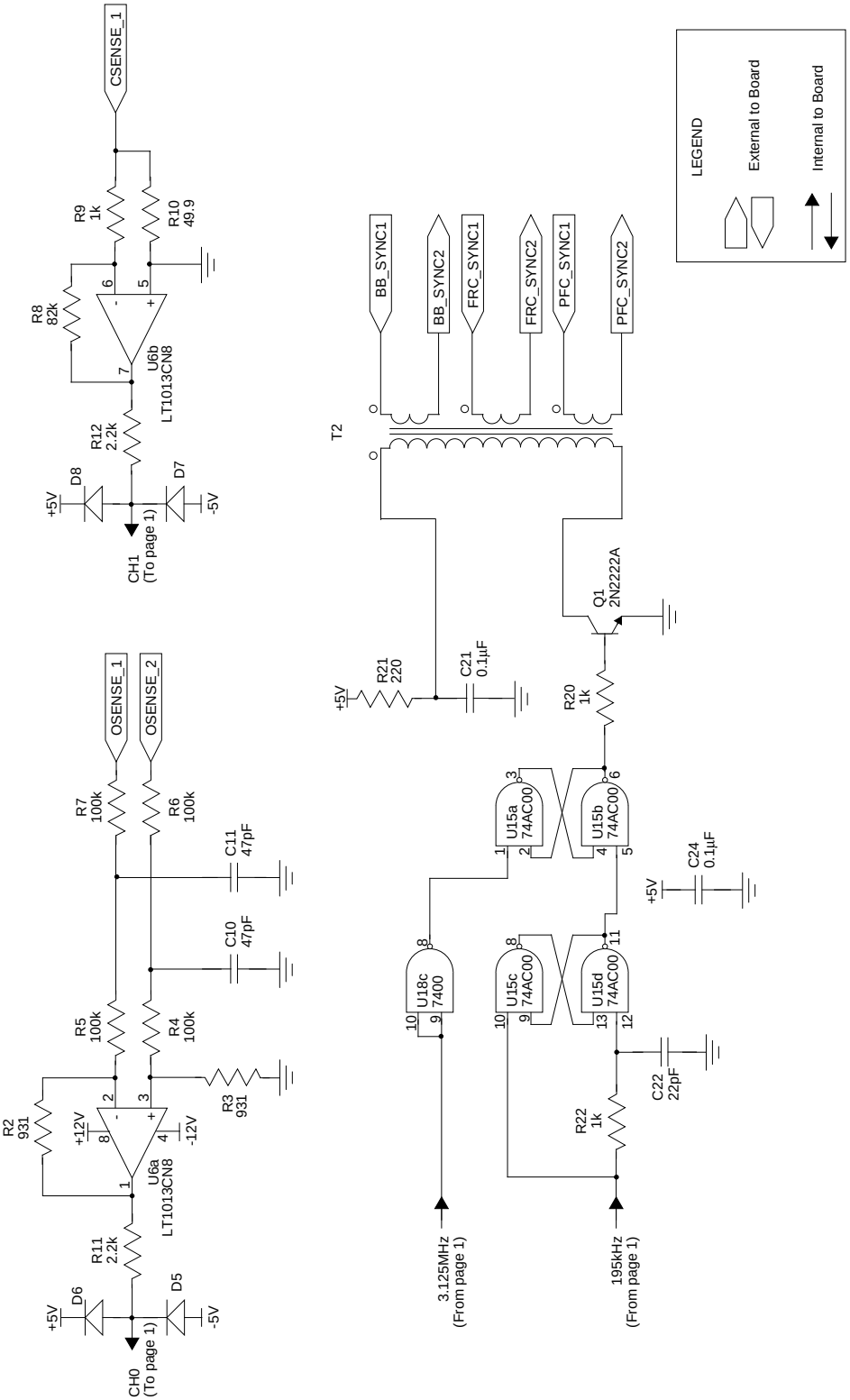


FIGURE B-6: INV CRTL – PAGE 3 OF 4

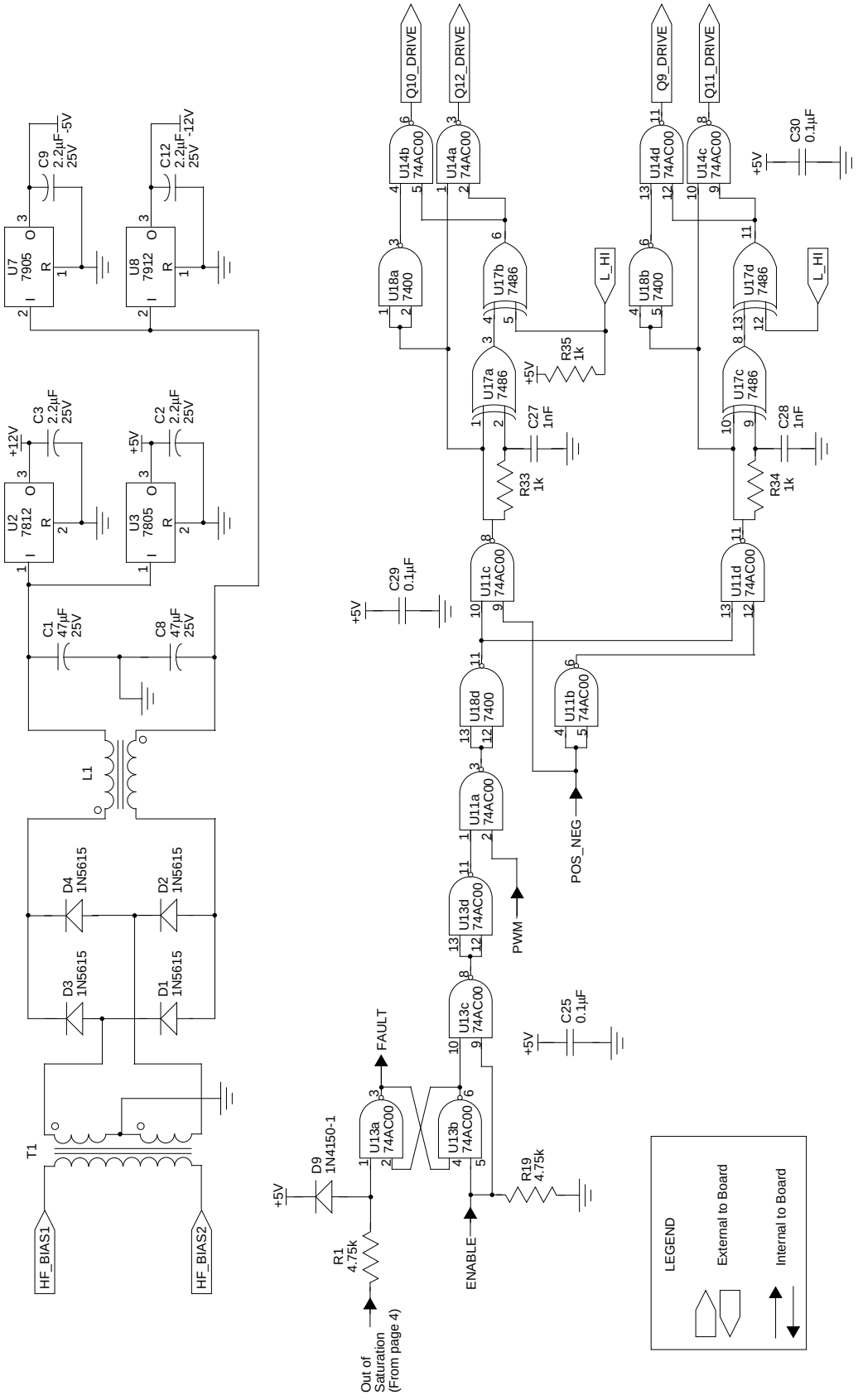


FIGURE B-6: INV CRTL – PAGE 4 OF 4

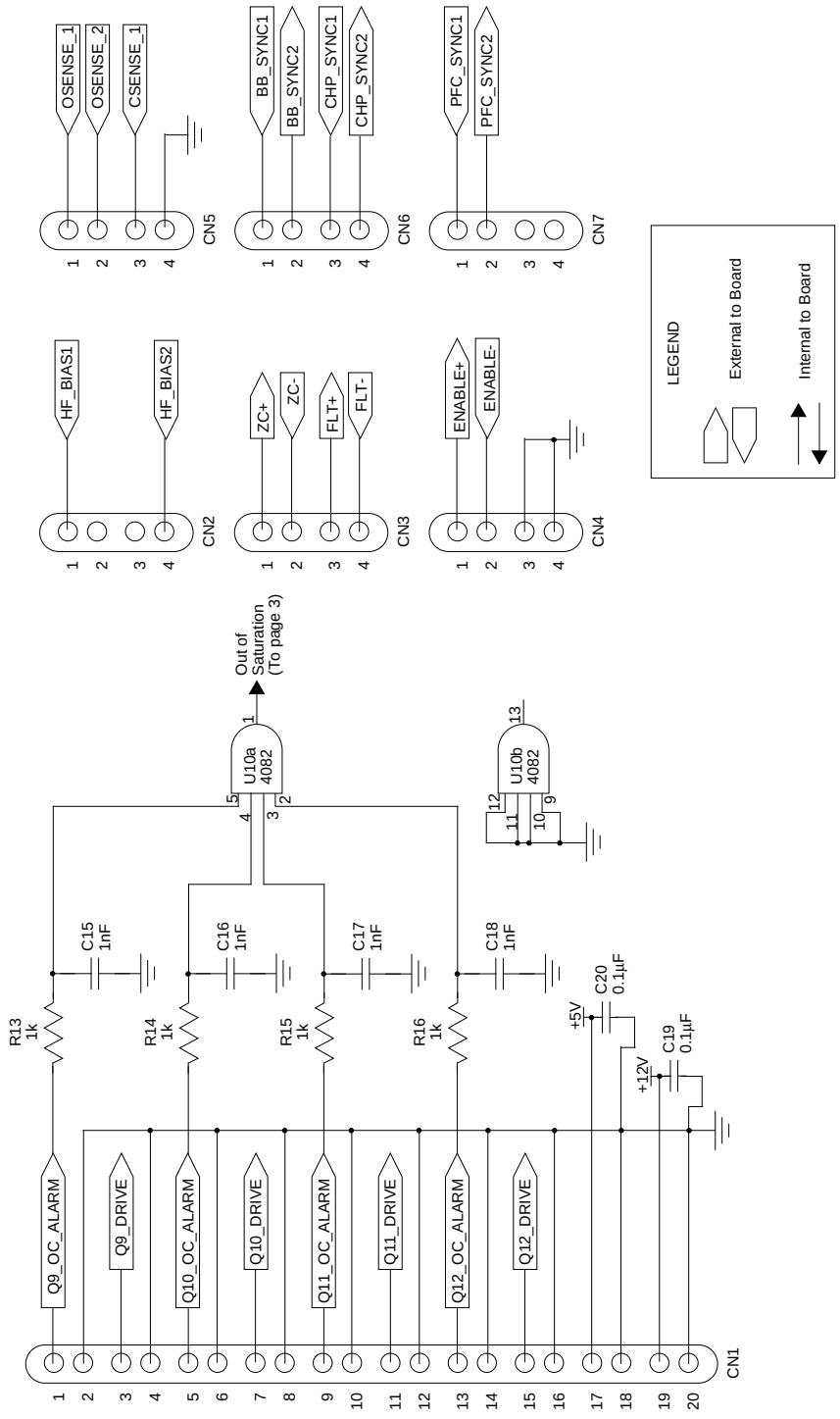
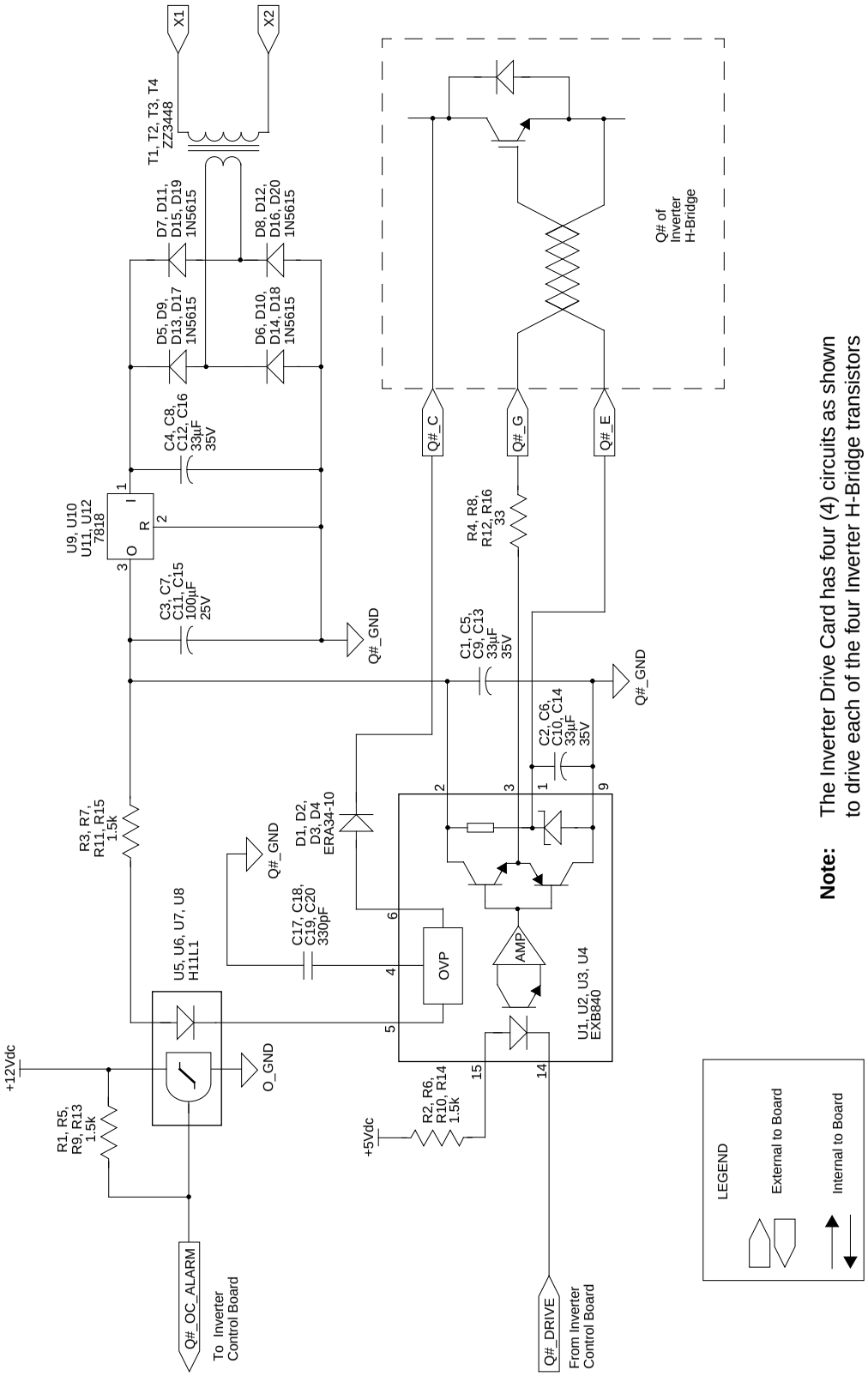
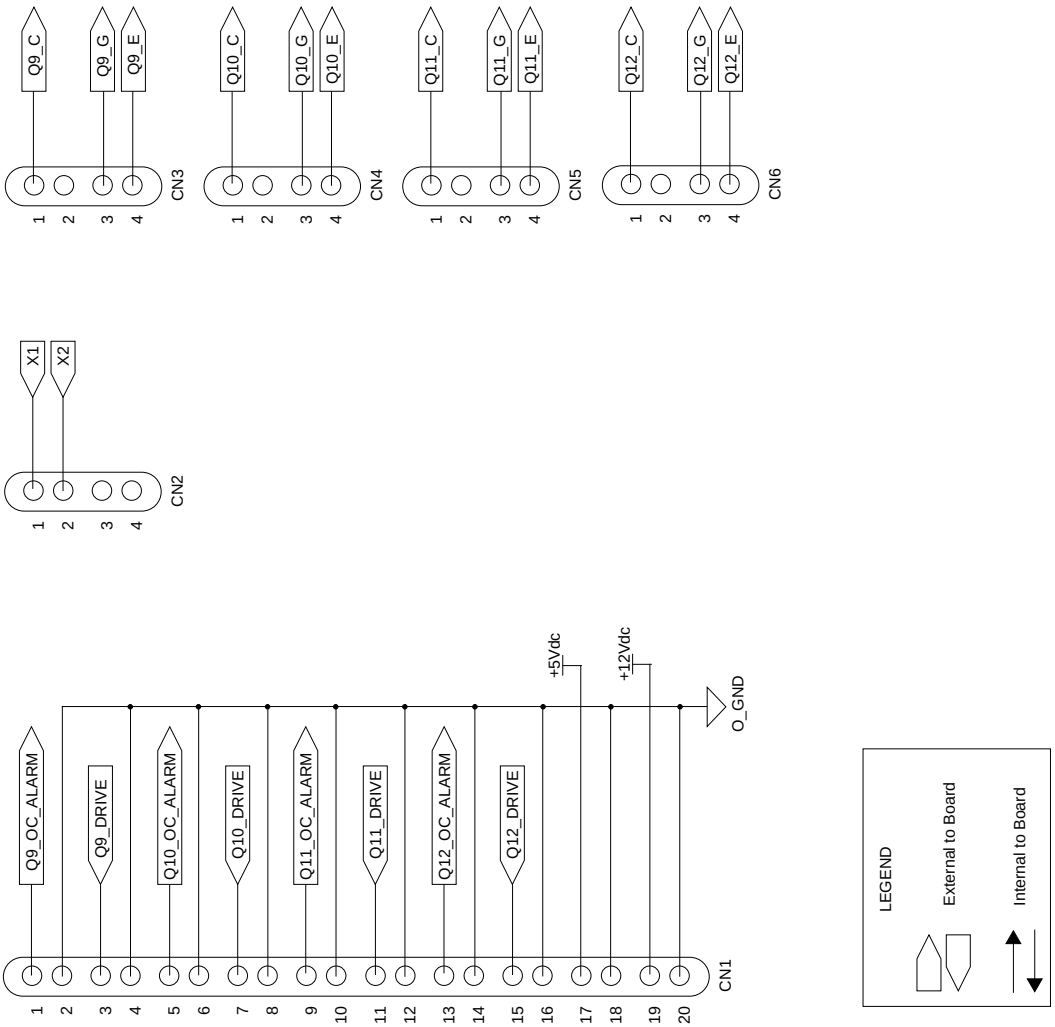


FIGURE B-7: INVERTER DRIVE (INV DRV) CARD – PAGE 1 OF 2



Note: The Inverter Drive Card has four (4) circuits as shown to drive each of the four Inverter H-Bridge transistors (# = 9, 10, 11, 12).

FIGURE B-7: INV DRV – PAGE 2 OF 2



APPENDIX C: SOFTWARE LISTING

The main purpose of the microcontroller software is to provide an inverter fast feedback loop response, such that the transient response and output distortion are that of a high performance design.

In addition, the inverter software may be used to provide the necessary communication to any “housekeeping” code as well as synchronization of the output voltage to the input voltage waveform. The housekeeping software was not developed for this reference design; however, the inverter software has “hooks” in place for such interfacing.

Housekeeping software should provide an overview control of the UPS power stream as well as the necessary communication and test functions to the outside world (i.e., on-board LCD display and host computer software interface).

The PICREF-1 software source code, as it existed at the time this document was published, is listed below. The most current version of PICREF-1 software may be obtained electronically on the Microchip BBS and WWW site.

```
/************************************************************************
*     Filename:     MAIN.C
************************************************************************
*
*     Author:      Dave Karipides
*     Company:     APS, Inc.
*     Date:        3-3-97
*     Compiled Using MPLAB-C Rev 1.21
*
************************************************************************
*
*     Include Files:
*
************************************************************************
*
*     Description:   The main routine calls all the functions for generating
*                    an OPEN_LOOP or FEEDBACK sine wave of either 50 or 60 Hz.
*
************************************************************************
*
*     Revisions:
*               3/3/97 Added FEEDBACK LOOP
*
*
************************************************************************/

/************************************************************************
*     main()
*
*     Description:   The main routine initializes the registers and loops
*                    forever.  All control is handled in the TMR0 INT
*                    routine.
*
*
*     Input Variables: NONE
*
*     Output Variables: NONE
*
*
************************************************************************/

//#define OPEN_LOOP
#define FEEDBACK
//#define 50Hz
#define 60Hz

#pragma option v
#include <17c43.h>
#include <math.h>
#include <delay16.h>

#ifdef OPEN_LOOP
```

```
// This table yields Full VRMS input
unsigned char const pwmtab[32]={0,25,50,74,98,120,142,162,180,197,212,
                    225,235,244,250,254,255,254,250,244,235,
                    225,212,197,180,162,142,120,98,74,50,25};
#endif
#ifdef FEEDBACK
// This table yields slightly less than Full VRMS input
unsigned char const pwmtab[32]={0,20,40,60,79,97,114,131,145,159,171,
                    181,189,197,202,205,206,205,202,197,189,
                    181,171,159,145,131,114,97,79,60,40,20};
#endif

long read_ad(unsigned char);    // Prototype for A/D converter function

unsigned char index;            // Index into the sinewave reference table
unsigned char sign;             // Flag used to unfold sinewave reference table
long reference;                 // Value of the sinewave refrence after unfolding
unsigned char reference_lo  @ reference; // V1.21 of Compiler does not type cast unsigned
                                // char to long so we will write to low byte separately
long out_volt;                  // Magnitude of the output voltage;
long y;                         // Variables used in compensation routine
long yold;
long x;
long xold;
long ad_value;                  // A/D Converter Value

void main(void)
{
     CLRWDT();
     PORTC = 0;          // Zero out portc latches
     DDRC = 0x22;        // Set up Data direction register for C
     DDRB = 0;           // Set up Data direction register for B
     PR1 = 0xFF;         // Setup PR1 register (24.4Khz @ 25Mhz clk)
     PW1DCL = 0;         // Set low bits of PWM to 0
     PW1DCH = 0;         // Init PWM duty cycle to 0

     T0STA = 0x20;       // Configure Timer0 prescaler
     INTSTA.T0IE = 1;    // Enable Timer 0 interrupt
     TCON1.TMR1CS = 0;
     TCON1.T16 = 0;
     TCON2.TMR1ON = 1;   // Start timer 1 (PWM timer)
     TCON2.PWM1ON = 1;   // Turn on the PWM
     CPUSTA.GLINTD = 0;  // Unmask the interrupts

     index = 0;          // Initialize variables
     sign = 0;
     y = 0;
     yold = 0;
     x = 0;
     xold = 0;
     PORTC.0 = 1;        // Enable the Inverter
     while(1);           // Loop forever, execute in INT Routine
}

#ifdef FEEDBACK
__TMR0()                 // Timer  interrupt
{
     T0STA.T0CS = 0;     // Stop timer
PORTB.7=1;
#ifdef 60Hz
     TMR0L=0xA5;
     TMR0H=0xF9;         // Make Timer0 interrupt at 3.84KHz for 60Hz output
#endif
#ifdef 50Hz
     TMR0L=0x5F;         // Make Timer0 interrupt at 3.20KHz for 50Hz output
     TMR0H=0xF8;
```

```
#endif
     T0STA.T0CS = 1;                 // Start timer
     CLRWDT();

     reference = 0;                  // Clear Reference Value
     reference_lo = pwmtab[index];   // Lookup the value of the sinewave reference

     if (!index)                     // Toggle Sign Every Cycle Through table
          sign = ~sign;
     ++index;                        // Increment index
     if (index == 32)                // If end of table, reset counter
          index = 0;
     if (sign)                       // If negative going wave
     {
          reference = ~reference;    // V1.21 of Compiler negate (-ref) doesn't work for
          reference = reference + 1; // ref<=0
     }
     ad_value = read_ad(0);
     out_volt = ad_value - 512;      // Read output voltage (512 counts=0 volts out)

// Form the expression y = yold + (0.09261 * (x + xold))
// Where yold, xold is the value of y, x from the previous sample
// x is the <error signal>, formed by the difference between the output
// of the inverter and the reference signal.
     x = out_volt - reference;
     y = ((x + xold) * 24);
     y = y / 256;
     y = y + yold;
     if (y >= 0)
     {
          PORTC.2 = 0;               // Set positive going cycle
     } else
     {
          PORTC.2 = 1;               // Set negative going cycle
          y = ~y;
          y = y + 1;
     }
     if (y > 255)
          y = 255;                   // Limit y
     PW1DCH = y;                     // Update duty cycle
     xold = x;                       // Store previous sample's state
     yold = y;
PORTB.7=0;
 }
#endif

#ifdef OPEN_LOOP
// The inverter runs in an open loop mode with OPEN_LOOP defined.
__TMR0()                       // Timer interrupt
{
     T0STA.T0CS = 0;           // Stop timer
#ifdef 60Hz
     TMR0L=0xA5;
     TMR0H=0xF9;               //Make Timer0 interrupt at 3.84KHz for 60Hz output
#endif
#ifdef 50Hz
     TMR0L=0x5F;               //Make Timer0 interrupt at 3.20KHz for 50Hz output
     TMR0H=0xF8;
#endif
     T0STA.T0CS=1;             //Start timer
     CLRWDT();

     PW1DCH = pwmtab[index];
     if (!index)
     {
          PORTC.0 = 0;         // Gate Drive off
```

```
          PORTC.2 = ~PORTC.2;     // Flip Pos/Neg bit
          PORTC.0 = 1;            // Gate Drive on
     }
     ++index;
     if (index == 32)
          index = 0;
     PORTC.3 = ~PORTC.3;          // Toggle bit to test freq.
}
#endif

long read_ad(unsigned char channel)
{
long result;

     PORTC.6 = 1;            // Write bit high
     PORTC.7 = 1;            // Read bit high
     PORTC.4 = 1;            // Chip select high
     DDRD = 0;               // Make PORTD an output
     PORTD = 0x04;           // Single ended mode signed 10 bit chan 0 Right justified
     PORTC.4 = 0;            // Select chip
     PORTC.6 = 0;            // latch command word int A/D
     PORTC.6 = 1;            // Start conversion
     PORTC.4 = 1;            // Deselect chip
     while (PORTC.5);        // Wait for conversion to complete
     DDRD = 0xFF;            // Make PORTD an input
     PORTC.4 = 0;            // Select chip
     PORTC.7 = 0;            // Read high byte
     *( ((unsigned char*)&result) + 1) = PORTD;
     PORTC.7 = 1;
     PORTC.4 = 1;
     PORTC.4 = 0;
     PORTC.7 = 0;            // Read low byte
     *( ((unsigned char*)&result) ) = PORTD;
     PORTC.7 = 1;
     PORTC.4 = 1;            // Reset chip select lines
     return (result);        // Return data
}
```

APPENDIX D: PCB LAYOUT & FAB DRAWING

Top silk screen drawings for the UPS control cards are shown in the following sections. The board dimensions listed are, with respect to the orientation of this page; (horizontal dimension x vertical dimension).

The boards shown are:

- Battery Boost PCB
- Free Running Chopper PCB
- Inverter Drive Card
- Inverter Control Card.

The Power Factor Correction circuit was not built up onto a board.

These drawings, and additional layout and fab drawings (top and bottom copper, top and bottom solder masks, drill drawings, report drawings and board drawings), may be obtained electronically on the Microchip BBS or WWW site.

FIGURE D-1: BATTERY BOOST PCB

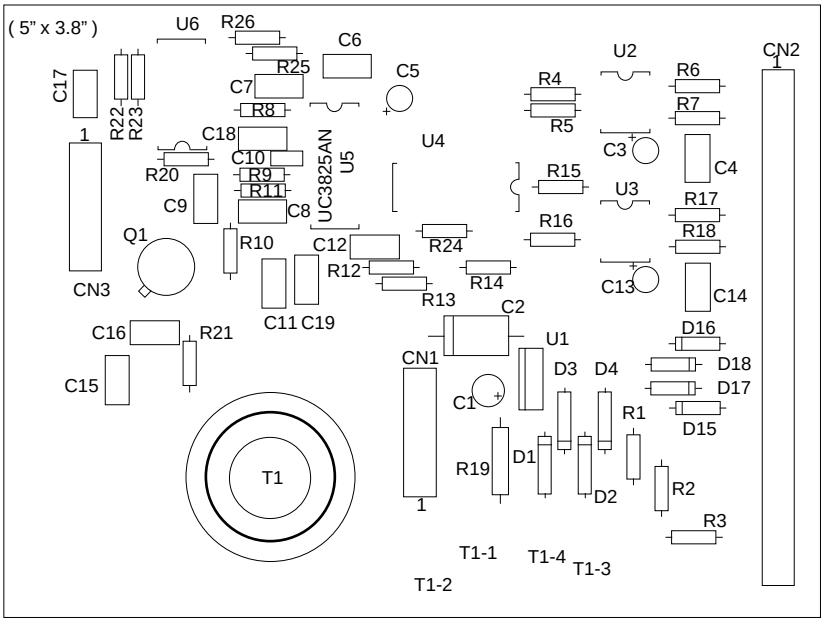


FIGURE D-2: FREE RUNNING CHOPPER PCB

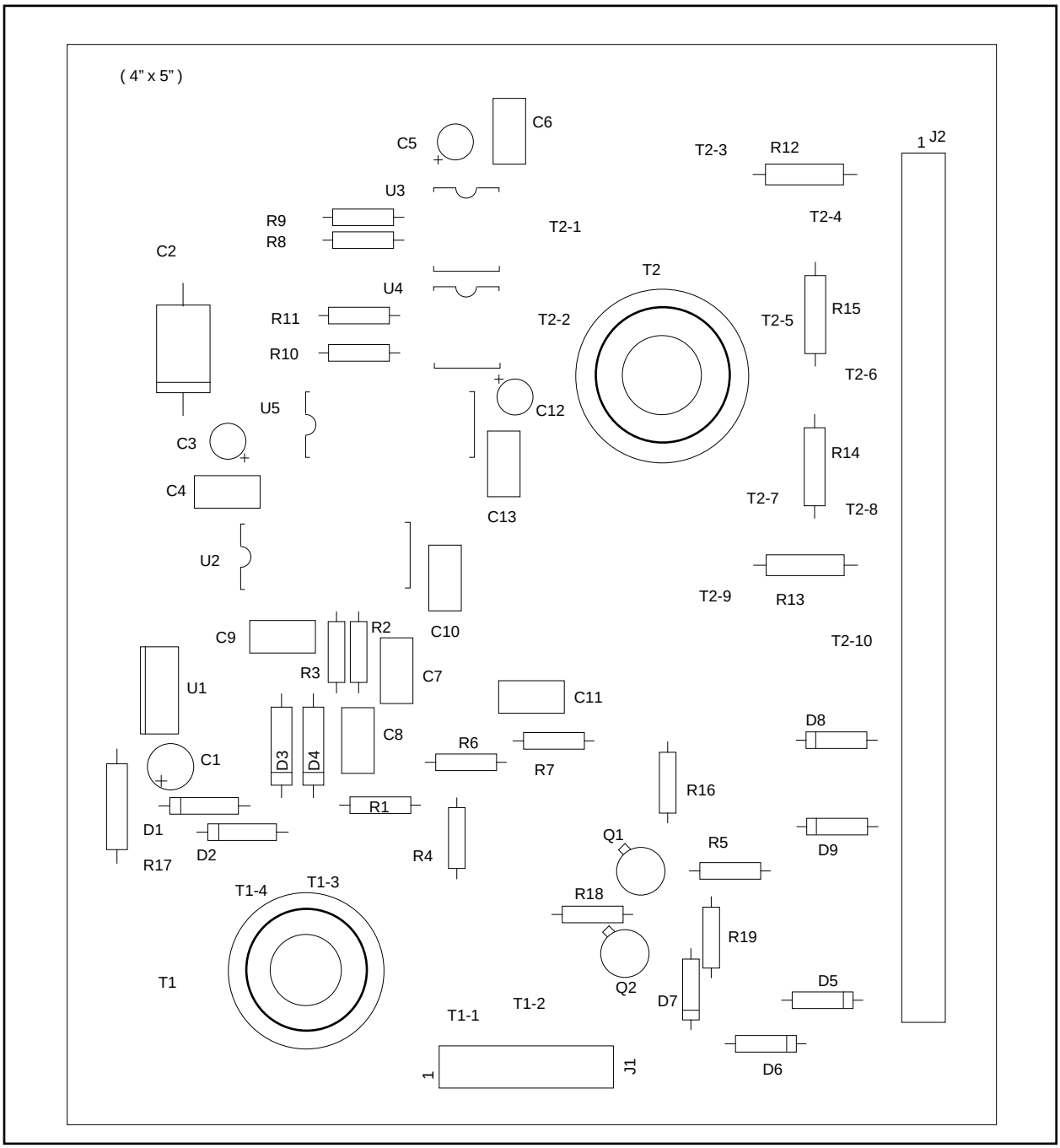


FIGURE D-3: INVERTER DRIVE CARD

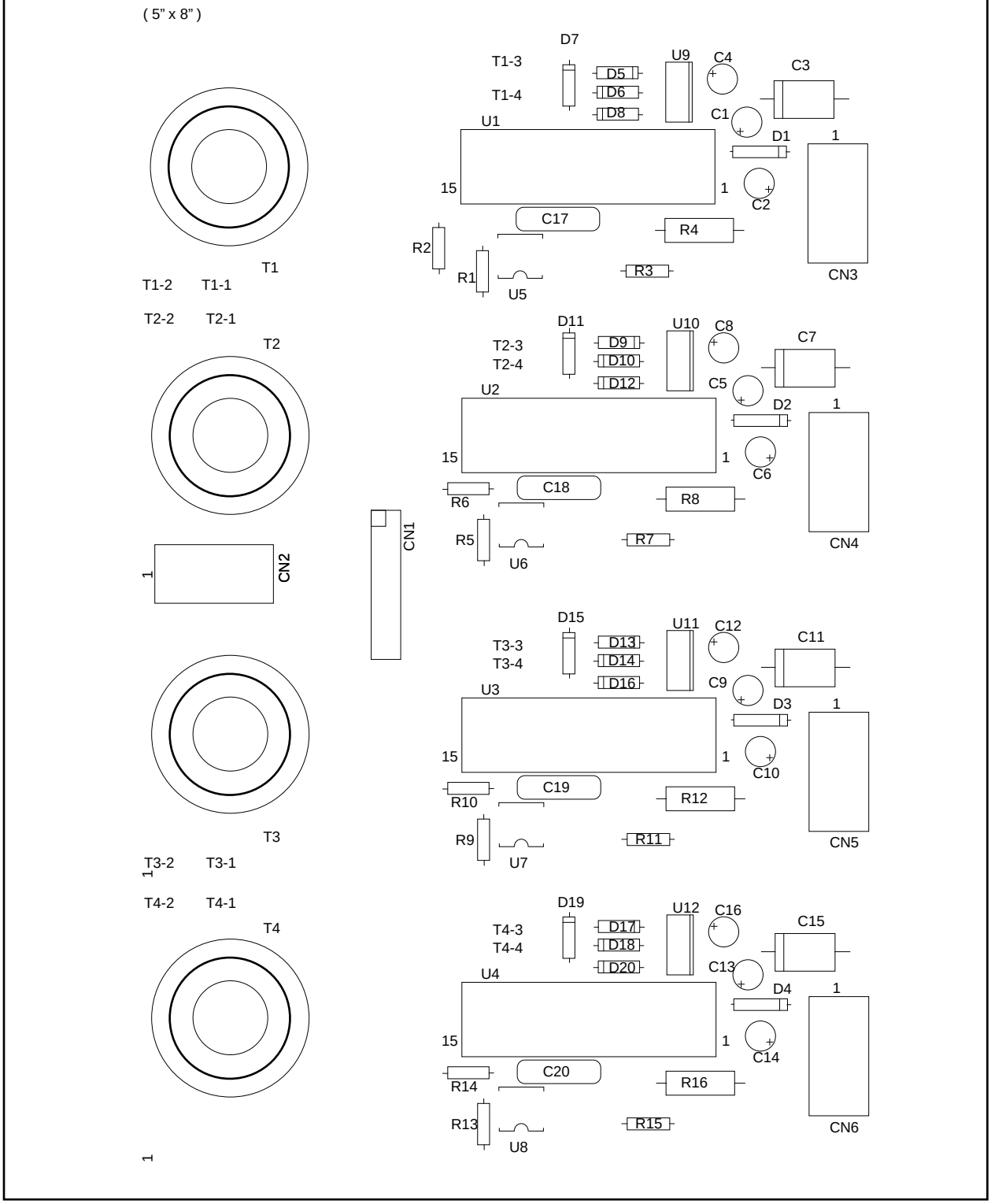
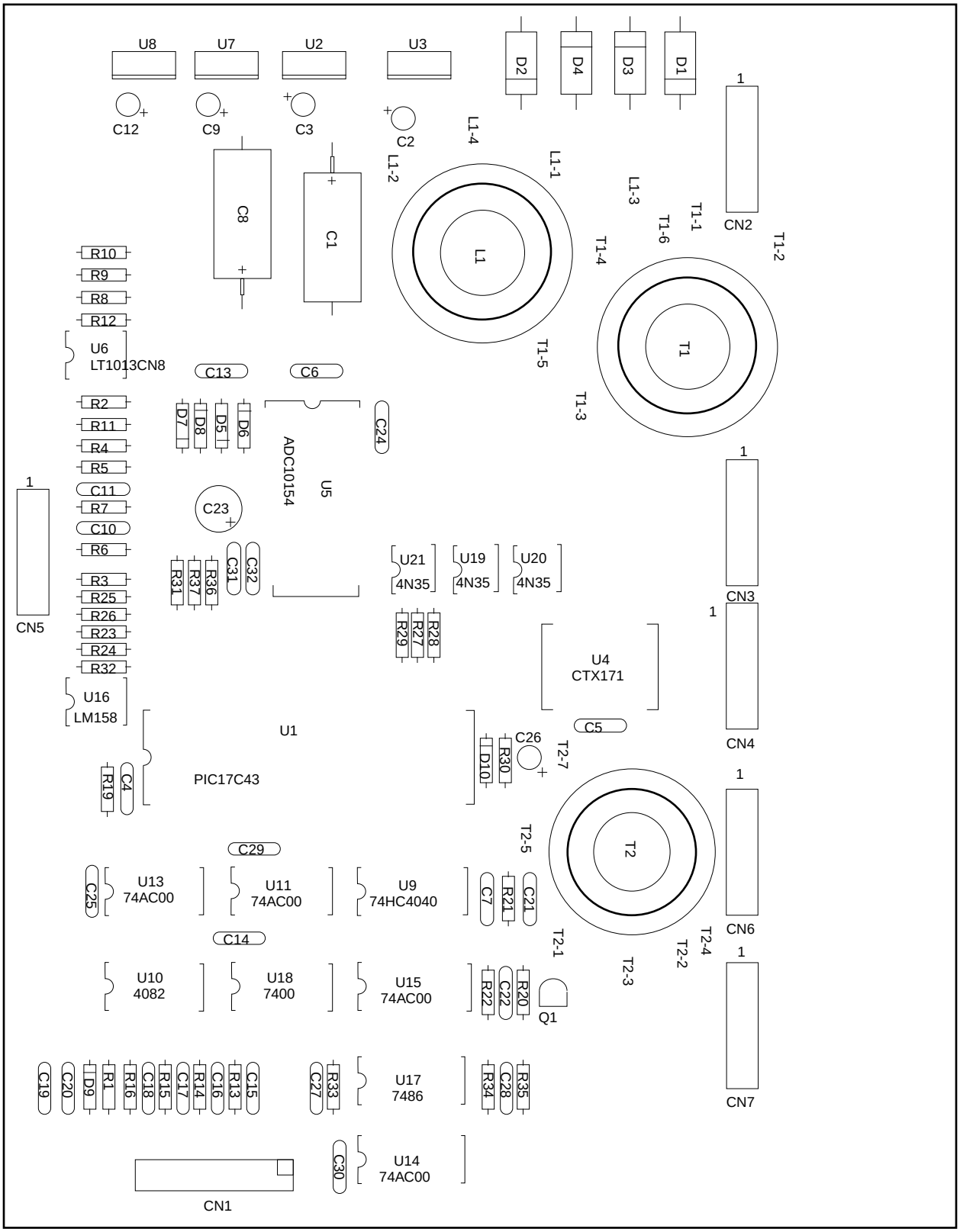


FIGURE D-4: INVERTER CONTROL CARD



APPENDIX E: BILL OF MATERIALS (BOM)

This appendix lists the Bill of Materials (BOM) for the UPS system assembly and for each of the UPS boards described in Appendix D.

E.1 UPS System Assembly

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Transistor	4	Q1 - Q4	IRFP264, International Rectifier, (310) 322-3331
Transistor	4	Q5 - Q8	IRF450, International Rectifier, (310) 322-3331; or Generic 2N6770
Transistors, 2 to a block, 75A	2	Q9 - Q12	2MBI75L-060, Fuji, (408) 922-9000; or CM75DY-12H, Powerex, (412) 925-7272 (800) 451-1415 (USA only)
Transformer	1	T1	ZZ3449, Airborne Power See *Acknowledgments* for email address
Transformer, current	1	T2	ZZ3450, Airborne Power See *Acknowledgments* for email address
Transformer	2	T4, T5	ZZ9454, Airborne Power See *Acknowledgments* for email address
Transformer	1	T6	ZZ3455, Airborne Power See *Acknowledgments* for email address
Transformer	1	T7	ZZ3459, Airborne Power See *Acknowledgments* for email address
Inductor, 500uH	1	L1	ZZ3451, Airborne Power See *Acknowledgments* for email address
Inductor, 725uH	1	L4	ZZ3456, Airborne Power See *Acknowledgments* for email address
Inductor, 300uH	2	L5, L6	ZZ3457, Airborne Power See *Acknowledgments* for email address
Inductor, 50uH	1	L7	ZZ3458, Airborne Power See *Acknowledgments* for email address
Switch	2	RLY1, RYL2	
Diode	3	D1, D2, D3	DESI 30-12A
Diode	2	D9, D10	DESI 60-12A
Capacitor, 1uF, 600V	3	C1, C4, C9	Generic
Capacitor, Electrolytic, 6100uF, 350V	2	C5, C6	Generic
Capacitor, Electrolytic, 250uF, 350V	2	C10, C11	Generic
Capacitor, 0.58uF	2	C12, C13	Generic
Capacitor, 10uF, 600V	4	C14 - C17	Generic
Resistor, 100kΩ, 2W	4	R4 - R7	Generic
Resistor, 5.6Ω	1	R8	Generic

E.2 Battery Boost PCB

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Cap, Ceramic 0.01µF, Radial Lead	3	C9,16,17	ECU-S1J103KBA, Panasonic (714) 373-7366
Cap, Ceramic 0.1µF, Radial Lead	1	C15	ECU-S2A104KBA, Panasonic (714) 373-7366
Cap, Ceramic .47µF, Radial Lead	3	C4, 6, 14	ECU-S1J474KBB, Panasonic (714) 373-7366
Cap, Tantalum 1.5µF, 25V, Radial Lead	4	C3, 5, 13, 18	ECS-F1EE155K, Panasonic (Digikey: P2044-ND) (714) 373-7366
Cap, Electrolytic 33µF, 35V, Axial Lead	1	C1	ECE-A1VU330, Panasonic (714) 373-7366
Cap, Electrolytic 100µF, 25V, Axial Lead	1	C2	ECE-B1EU101Y, Panasonic (714) 373-7366
Cap, Ceramic 100pF, Radial Lead	1	C10, 19	ECU-S2A101JCA, Panasonic (714) 373-7366
Cap, Ceramic 470pF, Radial Lead	2	C7, 11	ECU-S2A471JCB, Panasonic (714) 373-7366
Cap, Ceramic 680pF, Radial Lead	1	C12	ECU-S2A681JCB, Panasonic (714) 373-7366
Cap, Ceramic 2700pF, Radial Lead	1	C8	ECU-S2A272JCB, Panasonic (714) 373-7366
Terminal Block, Wire-to-PCB Stackable, 200mil	12	CN1, 2, 3	ED120/2DS, On-Shore Technology (602) 921-3000
Diode, Small-signal, Axial Lead	4	D15,16,17,18	1N4150-1, Microsemi (602) 244-6900
Diode, Fast-Recovery, 200V, 1A, Axial Lead	4	D1-4	1N5615, Microsemi (602) 244-6900
Transistor, Small-signal, NPN, TO-18	1	Q1	2N2222A, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
Resistor, 5.6Ω, 1/4 Watt, Axial Lead	4	R6, 7, 17,18	Generic
Resistor, 6.2Ω 1/4 Watt, Axial Lead	1	R14	Generic
Resistor, 24Ω, 1/4 Watt, Axial Lead	1	R10	Generic
Resistor, 47Ω, 1/2 Watt, Axial Lead	1	R19	Generic
Resistor, 100Ω, 1/4 Watt, Axial Lead	1	R20	Generic
Resistor, 510Ω, 1/4 Watt, Axial Lead	1	R12	Generic
Resistor, 523Ω, 1/4 Watt, Axial Lead	1	R1	Generic
Resistor, 1kΩ, 1/4 Watt, Axial Lead	3	R 5, 13, 16	Generic
Resistor, 2kΩ, 1/4 Watt, Axial Lead	2	R4, 15	Generic
Resistor, 2.67kΩ, 1/4 Watt, Axial Lead	1	R9	Generic
Resistor, 6.8kΩ, 1/4 Watt, Axial Lead	1	R11	Generic
Resistor, 10.4kΩ, 1/4 Watt, Axial Lead	3	R8, 21, 22	Generic
Resistor, 35.7kΩ, 1/4 Watt, Axial Lead	1	R2	Generic
Resistor, 37.5kΩ, 1/4 Watt, Axial Lead	1	R3	Generic
Resistor, 69.8kΩ, 1/4 Watt, Axial Lead	1	R23	Generic
Transformer	1	T1	ZZ3448, Airborne Power See *Acknowledgments* for email address

E.2 Battery Boost PCB (Continued)

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
IC, Hex Inverter 14-PIN DIP	1	U4	MC14049UBCL, Motorola (602) 244-6900
IC,+15V Voltage Regulator TO-220	1	U1	MC7815CT, Motorola (602) 244-6900
IC, Quad Comparator 14-PIN DIP	1	U6	LM339N, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
IC, Driver, Line, 8-PIN DIP	2	U2, 3	TSC429CPA, TelCom (415) 968-9241 (800) 888-9966 (USA Only)
IC, PWM, 18-PIN DIP	1	U5	UC3825AN, Unitrode (603) 429-8610

E.3 Free Running Chopper PCB

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Cap, Ceramic .47µF, Radial Lead	3	C4, 6, 13	ECU-S1J474KBB, Panasonic (714) 373-7366
Cap, Tantalum 1.5µF, 25V, Radial Lead	3	C3, 5, 12	ECS-F1EE155K, Panasonic (714) 373-7366
Cap, Electrolytic 33µF, 35V, Radial Lead	1	C1	ECE-A1VU330, Panasonic (714) 373-7366
Cap, Electrolytic 100µF, 25V, Axial Lead	1	C2	ECE-B1EU101Y, Panasonic (714) 373-7366
Cap, Ceramic 100pF, Radial Lead	1	C9	ECU-S2A101JCA, Panasonic (714) 373-7366
Cap, Ceramic 470pF, Radial Lead	1	C10	ECU-S2A471JCB, Panasonic (714) 373-7366
Cap, Ceramic 680pF, Radial Lead	1	C11	ECU-S2A681JCB, Panasonic (714) 373-7366
Cap, Ceramic 2200pF, Radial Lead	1	C8	ECU-S2A222JCB, Panasonic (714) 373-7366
Cap, Ceramic 4700pF, Radial Lead	1	C7	ECU-S1J472KBA, Panasonic (714) 373-7366
Terminal Block, Wire-to-PCB Dual-Stackable, 200mm spacing	12	CN1, 2	ED120/2DS, On-Shore Technology (602) 921-3000
Diode, Small-signal Axial Lead	2	D8, 9	1N4150-1, Microsemi (602) 244-6900
Diode, Fast Rectifier 200V, 1A, Axial Lead	4	D1-4	1N5615, Microsemi (602) 244-6900
Diode, Zener Axial Lead	3	D5-7	1N985B, Motorola (602) 244-6900
Transistor, Small-signal NPN, TO-18	2	Q1,2	2N2222A, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
Resistor, 12Ω, 1/4 Watt, Axial Lead	4	R12-15	Generic
Resistor, 20Ω, 1/4 Watt, Axial Lead	1	R16	Generic
Resistor, 24Ω, 1/4 Watt, Axial Lead	1	R1	Generic
Resistor, 100Ω, 1/4 Watt, Axial Lead	1	R4	Generic
Resistor, 510Ω, 1/4 Watt, Axial Lead	1	R7	Generic
Resistor, 1kΩ, 1/4 Watt, Axial Lead	3	R6, 9, 11	Generic
Resistor, 1.5kΩ, 1/4 Watt, Axial Lead	1	R3	Generic
Resistor, 1.78kΩ, 1/4 Watt, Axial Lead	1	R2	Generic
Resistor, 2.2kΩ, 1/4 Watt, Axial Lead	2	R8, 10	Generic
Resistor, 47Ω, 1/4 Watt, Axial Lead	1	R17	Generic
Resistor, 4.7kΩ, 1/4 Watt, Axial Lead	2	R18	Generic
Resistor, 10kΩ, 1/4 Watt, Axial Lead	1	R5	Generic
Resistor, 100kΩ, 1/4 Watt, Axial Lead	2	R19	Generic
Transformer Bias Supply	1	T1	TF5S03ZZ3448, Airborne Power See *Acknowledgments* for email address
Transformer Drive	1	T2	TF5S03ZZ3460, Airborne Power See *Acknowledgments* for email address
IC, Hex Inverter 14-Pin DIP	1	U5	MC14049UBCL, Motorola (602) 244-6900

E.3 Free Running Chopper PCB (Continued)

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
IC, +15V Voltage Regulator TO-220	4	U1	MC7815CT, Motorola (602) 244-6900
IC, Driver, Line 8-Pin DIP	2	U3, 4	TSC429CPA, TelCom (415) 968-9241 (800) 888-9966 (USA Only)
IC, PWM 18-Pin DIP	1	U2	UC3825AN, Unitrode (603) 429-8610

E.4 Inverter Drive Card

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Cap, Electrolytic, 33µF, 35V, Axial Lead	12	C1, 2, 4-6, 8-10, 12-14, 16	ECE-A1VU330, Panasonic (714) 373-7366
Cap, Film, 100µF, 25V, Axial Lead	4	C3, 7, 11, 15	ECE-B1EU101Y, Panasonic (714) 373-7366
Connector, Ribbon Cable, 20-position	1	CN1	3428-6002, 3M Scotchflex (512) 984-1800 (800) 225-5373 (USA Only)
Terminal Block, Wire-to-PCB, 2 Position Dual, 200mil spacing	10	CN2-6	ED120/2DS, On-Shore Technology (602) 921-3000
Diode, Fast Recovery, 600V, 1A, Axial Lead	4	D1-4	ERA34-10, Fuji (Collmer) (214) 233-1589
Diode, Fast-Recovery, 200V, 1A, Axial Lead	16	D5-20	1N5615, Microsemi (602) 244-6900
Resistor, 1/2 Watt, 33Ω, 1%, Axial Lead	4	R4, 8, 12, 16	Generic
Resistor, 1/4 Watt, 1.5kΩ, 1%, Axial Lead	12	R1-3, 5-7, 9-11, 13-15	Generic
Transformer, Toroid 100kHz, 24:27	4	T1-4	TF5S03ZZ3448, Airborne Power (Core is XJ-41605-TC) See *Acknowledgments* for email address
IC, Optocoupler, 6-Pin DIP Schmitt Trigger Logic-Output	4	U5-8	H11L1QT, QT Optoelectronics (214) 447-1304
Voltage Regulator, TO-220 18Vdc	4	U9-12	MC7818CT, Motorola (602) 244-6900
Driver, IGBT. Hybrid Package	4	U1-4	EXB840, Fuji (201) 712-0555
Retainer, Toroid	4		100-2, Delbert-Blinn (909) 629-3900
Screw, 4-40x1/2 ", Stainless Steel	4		Generic
Washer, 4-40", Stainless Steel	4		Generic

E.5 Inverter Control Card

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Cap, Ceramic, C0G 22pF, 100V, Radial Lead	1	C22	ECU-S2A220JCA, Panasonic (714) 373-7366
Cap, Ceramic, X7R 0.001µF, 100V, Radial Lead	8	C10, 11, 15-18, 27, 28	ECU-S2A102KBA, Panasonic (714) 373-7366
Cap, Ceramic, X7R 0.1µF, 100V, Radial Lead	15	C4-7, 13, 14, 19-21, 24, 25, 29, 30, 31, 32	ECU-S2A104KBA, Panasonic (714) 373-7366
Cap, Tantalum, 2.2µF, 25V, Axial Lead	4	C2, 3, 9, 12	ECS-F1EE225K, Panasonic (714) 373-7366
Cap, Electrolytic, 330µF, 16V, Radial Lead	1	C23	ECE-A1CU331, Panasonic (714) 373-7366
Cap, Electrolytic, 47µF, 25V, Axial Lead	2	C1, 8	ECE-B1EFS470, Panasonic (714) 373-7366
Cap, Tantalum, 4.7µF, 10V, Axial Lead	1	C26	ECS-F1AE475K, Panasonic (714) 373-7366
Connector, Ribbon Cable, 20-position	1	CN1	3428-6002, 3M Scotchflex (512) 984-1800 (800) 225-5373 (USA Only)
Terminal Block, Wire-to-PCB, 2 Position Dual-Stackable, 200mm spacing	12	CN2-7	ED120/2DS, On-Shore Technology (602) 921-3000
Diode, Small-signal, Axial Lead	6	D5-10	1N4150-1, Motorola (602) 244-6900
Diode, Fast Recovery, 200V, 1A, Axial Lead	4	D1-4	1N5615, Microsemi (602) 244-6900
Transistor, Small-signal, NPN, TO-18	1	Q1	2N2222A, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
Resistor, 1/4 Watt, 49.9Ω, 1%, Axial Lead	1	R10	Generic
Resistor, 1/4 Watt, 220Ω, 1%, Axial Lead	1	R21	Generic
Resistor, 1/4 Watt, 1kΩ, 1%, Axial Lead	13	R9, 13-16, 20, 22, 27-29, 33-35	Generic
Resistor, 1/4 Watt, 2.2kΩ, 1%, Axial Lead	2	R11, 12	Generic
Resistor, 1/4 Watt, 4.75kΩ, 1%, Axial Lead	8	R1, 19, 23-26, 31, 32	Generic
Resistor, 1/4 Watt, 932kΩ, 1%, Axial Lead	2	R2, 3	Generic
Resistor, 1/4 Watt, 82kΩ, 1%, Axial Lead	1	R8	Generic
Resistor, 1/4 Watt, 100kΩ, 1%, Axial Lead	4	R4-7	Generic
Inductor, Toroid	1	L1	TF5S04ZZ3461, Airborne Power See *Acknowledgments* for email address
Transformer, Toroid 1P/2S CT'ed	1	T1	TF5S03ZZ3462, Airborne Power See *Acknowledgments* for email address
Transformer, Toroid 1P/1S	1	T2	TF5S36ZZ3463, Airborne Power See *Acknowledgments* for email address
IC, 18-bit Shift Register, 16-Pin DIP	1	U9	MC14040BAP, Motorola (602) 244-6900
IC, +5V Voltage Regulator TO-220	1	U3	MC7805CT, Motorola (602) 244-6900
IC, -5V Voltage Regulator TO-220	1	U7	MC7905CT, Motorola (602) 244-6900

E.5 Inverter Control Card (Continued)

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
IC, +12V Voltage Regulator TO-220	1	U2	MC7812CT, Motorola (602) 244-6900
IC, -12V Voltage Regulator TO-220	1	U8	MC7912CT, Motorola (602) 244-6900
IC, Optocoupler 6-Pin DIP	3	U19-21	4N35QT, QT Optoelectronics (214) 447-1304
IC, Quad NAND Gates 14-Pin DIP	4	U11, 13-15, 18	74AC00PC, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
IC, A-D Converter, 24-Pin DIP	1	U5	ADC10154CIN, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
Oscillator, Clock 25MHz, (14-Pin DIP compatible)	1	U4	CTX171, CTS (815) 786-8411
IC, Op Amps Low-Power, Dual, 8-Pin DIP	1	U16	LM358AN, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
IC, Op Amp Precision, Dual, 8-Pin DIP	1	U6	LT1013CN8, Linear Technology (408) 432-1900
IC, Microcontroller 40-Pin DIP	1	U1	PIC17C43, Microchip Technology (602) 786-7200
IC, Dual 4-input AND Gate 14-Pin DIP	1	U10	CD4082BE, Harris (407)724-7000 (800) 4 HARRIS (USA Only)
IC, Quad 2-input Exclusive-OR Gate, 14-pin DIP	1	U17	74AC86PC, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)

APPENDIX F: UPS DEMO UNIT

The Demo Unit is a subset of the UPS. This unit was designed to showcase the inverter, featuring the PIC17C43 microcontroller. Therefore, there is no battery back-up circuitry.

AC power is filtered as it enters the UPS demo unit. There is also an input fuse to protect against surges. There is no power factor correction circuitry, and a rectifier-bridge is used to feed the inverter, or H-Bridge (i.e., no free-running chopper). There is output filtering and feedback circuitry.

The circuit boards used on the demo unit are the inverter drive PCB, the inverter control PCB and a bias supply board used to supply 15Vdc to the unit's discrete components.

F.1 Demo Specifications

The UPS demo specifications are the same as for the UPS system.

F.2 Demo Additional Schematics, PCB's, BOMs

FIGURE F-1: BIAS SUPPLY CIRCUIT

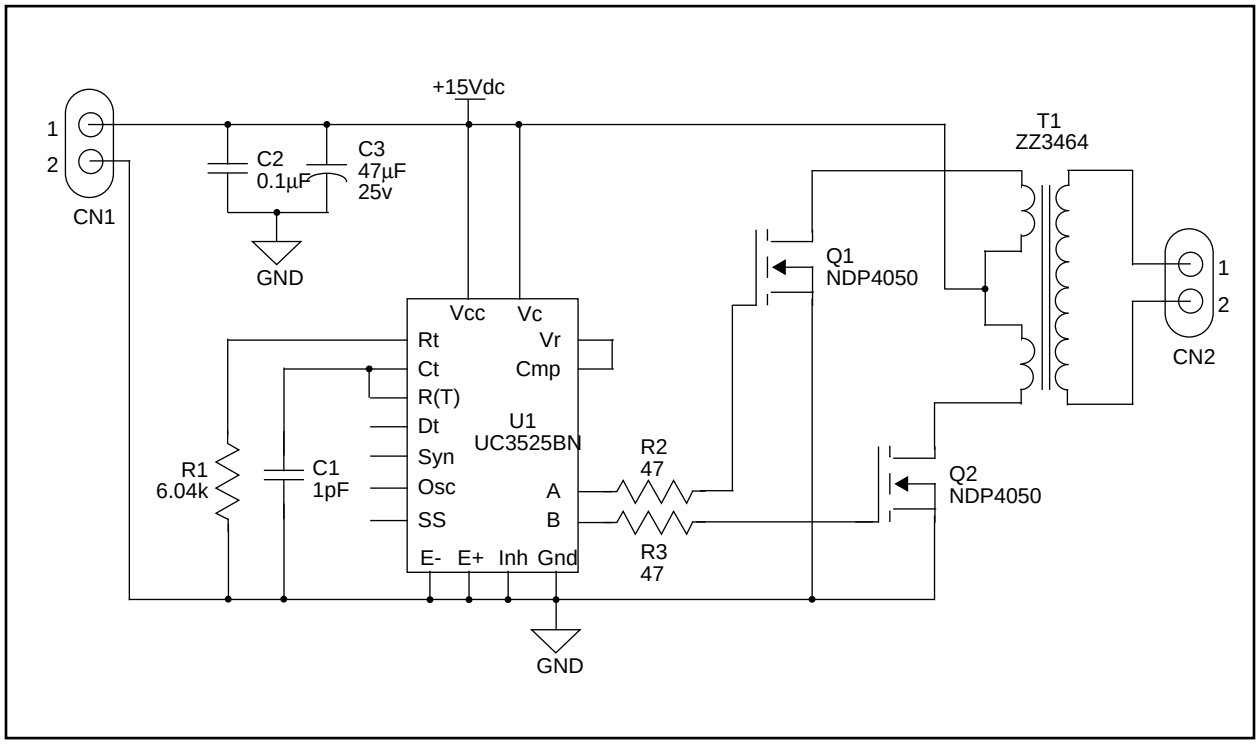


FIGURE F-2: BIAS SUPPLY BOARD

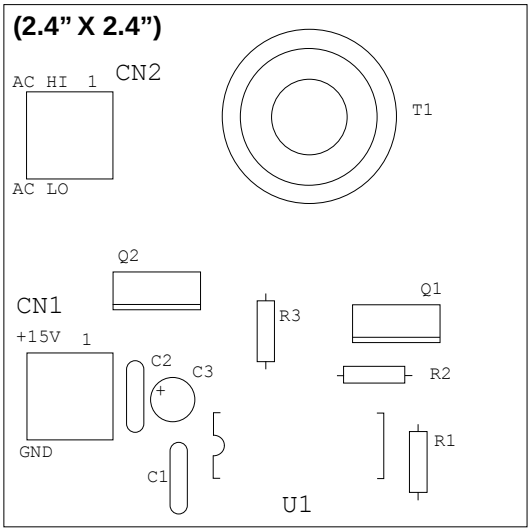


FIGURE F-3: RECTIFIER-BRIDGE CIRCUIT

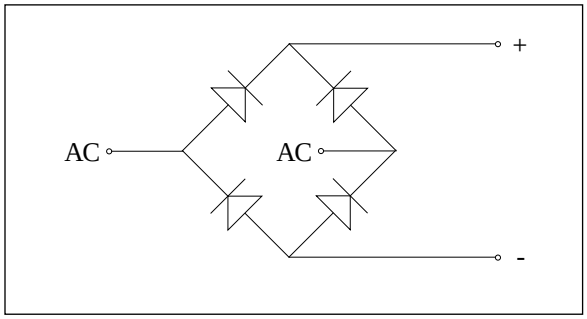


TABLE F-1: BIAS SUPPLY BOM

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Cap, Electrolytic, 47µF, 25V, Radial Lead	1	C3	ECE-A1EU470, Panasonic (714) 373-7366
Cap, Ceramic, .1µF, 63V, Radial Lead	1	C2	ECU-S1J104KBB, Panasonic (714) 373-7366
Cap, Ceramic, .001µF, 63V, Radial Lead	1	C1	ECU-S1J102JCB, Panasonic (714) 373-7366
Terminal Block, Wire-to-PCB, 2 Position Dual-Stackable, 200mil spacing	2	CN1,2	ED120/2DS, On-Shore Technology (602) 921-3000
Resistor, 1/4 Watt, 47Ω, 1%, Axial Lead	2	R2,3	Generic
Resistor, 1/4 Watt, 6.04KΩ, 1%, Axial Lead	1	R1	Generic
Transformer, Toroid 100KHz	1	T1	TF5S03ZZ3464, Airborne Power (Core XJ-41605-TC) See *Acknowledgments* for email address
IC, PWM, 16-Pin DIP	1	U1	UC3525BN, Unitrode (603) 429-8610
Transistor, TO-220 N-Chan, MOSFET, 50V	2	Q1,2	NDP4050, National Semiconductor (408) 712-5800 (800) 272-9959 (USA Only)
PCB, 2.4" x 2.4" Bias Supply, 100KHz	1		Generic PCB
Retainer, Toroid	1		100-2, Delbert-Blinn (909) 629-3900
Screw, 4-40x1/2 ", Stainless Steel	1		Generic
Washer, 4-40", Stainless Steel	1		Generic

TABLE F-2: OTHER BOM

DESCRIPTION	QTY	DESIGNATORS	PART #, MANUFACTURER, CONTACT #
Rectifier-Bridge Circuit	1		M5060SB1200, CRYDOM (818) 956-3900
Power Supply PCB	1		SW10-15PC, Toko America (847) 297-0070
Audio Transformer (On-Board Isolation Transformer)	1		705-0862, Allied (817) 595-3500 (800) 433-5700 (USA Only)

F.2.1 DEMO UNIT ASSEMBLY

DANGER

Electrocution Hazard
Do Not Disassemble Unit

A UPS Demo Unit is shown in different stages of assembly, for top and side aspects, in the figures below.

FIGURE F-4: DEMO PARTIAL ASSEMBLY - TOP VIEW

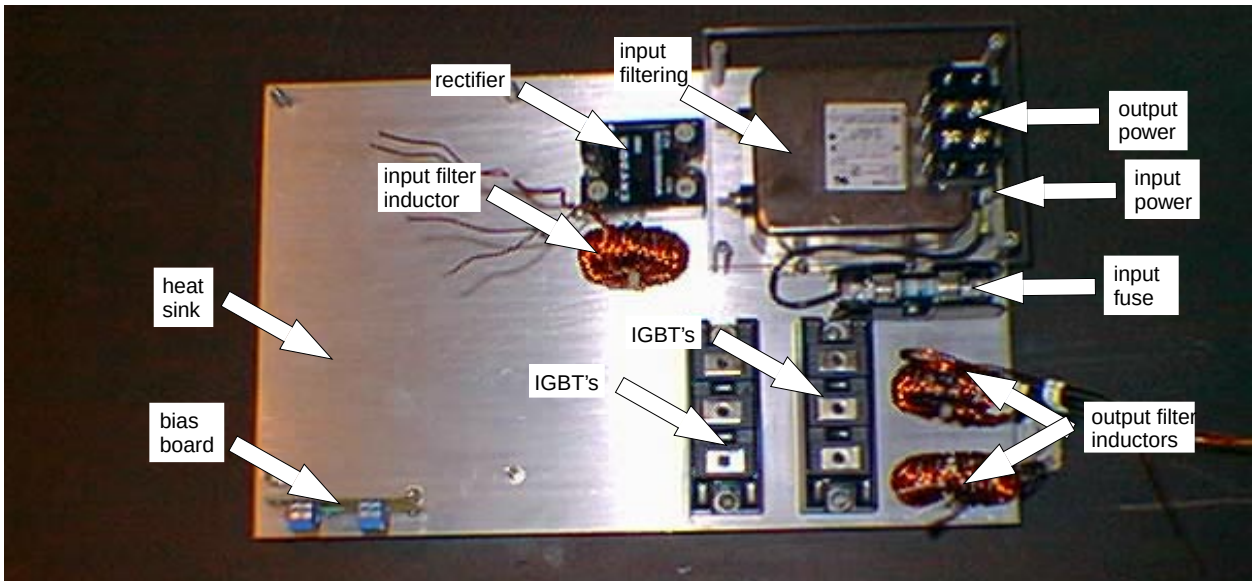


FIGURE F-5: DEMO FULL ASSEMBLY - TOP VIEW

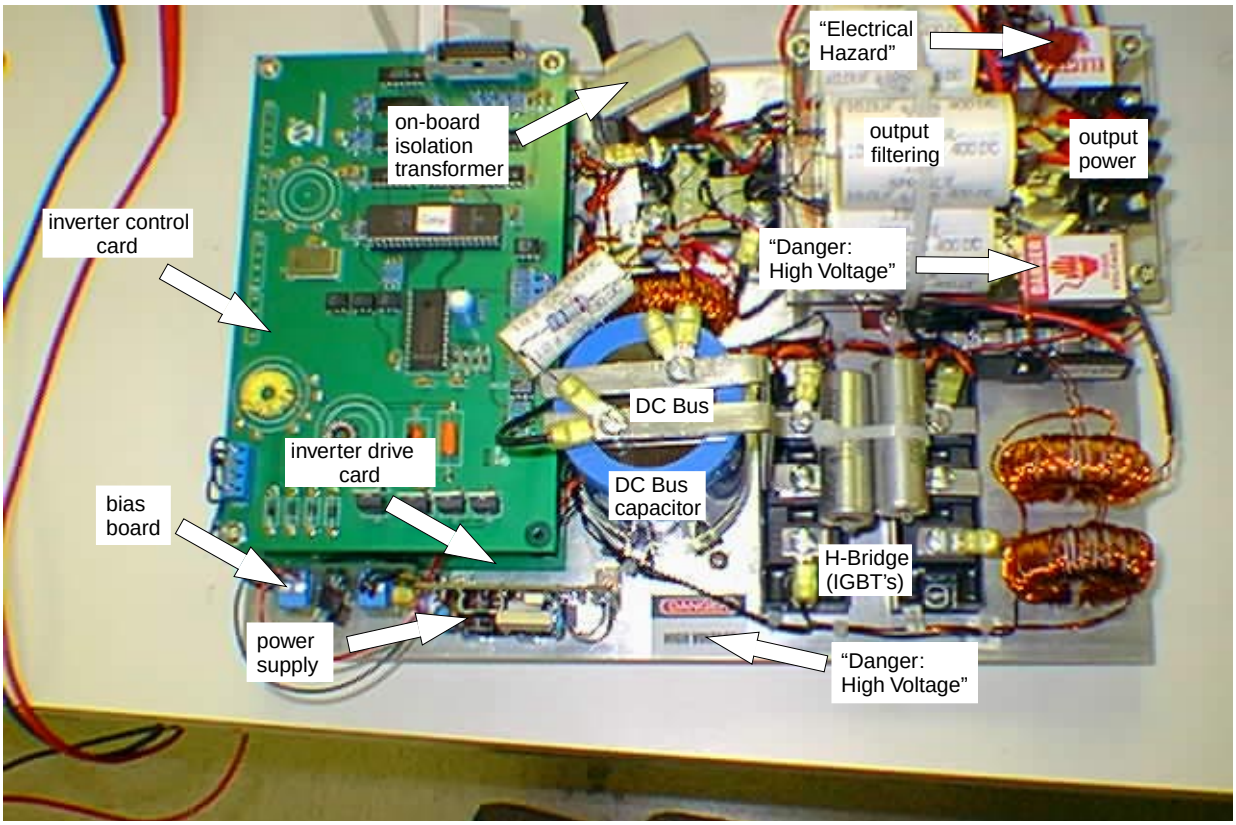


FIGURE F-6: DEMO PARTIAL ASSEMBLY - FRONT VIEW

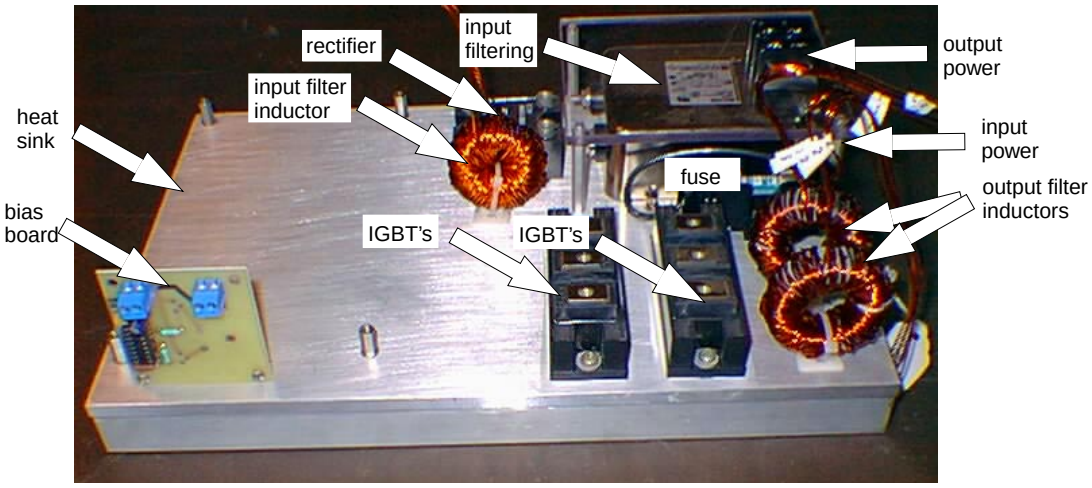


FIGURE F-7: DEMO FULL ASSEMBLY - FRONT VIEW

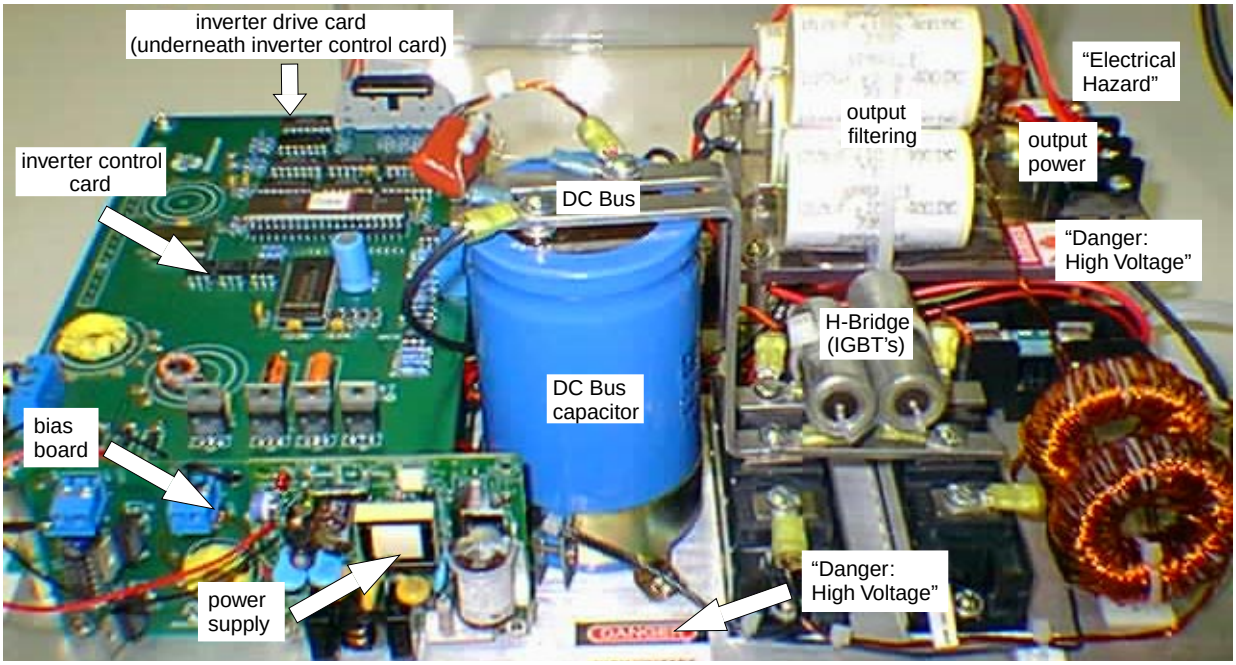


FIGURE F-8: DEMO PARTIAL ASSEMBLY - INVERTER CARDS DETAIL

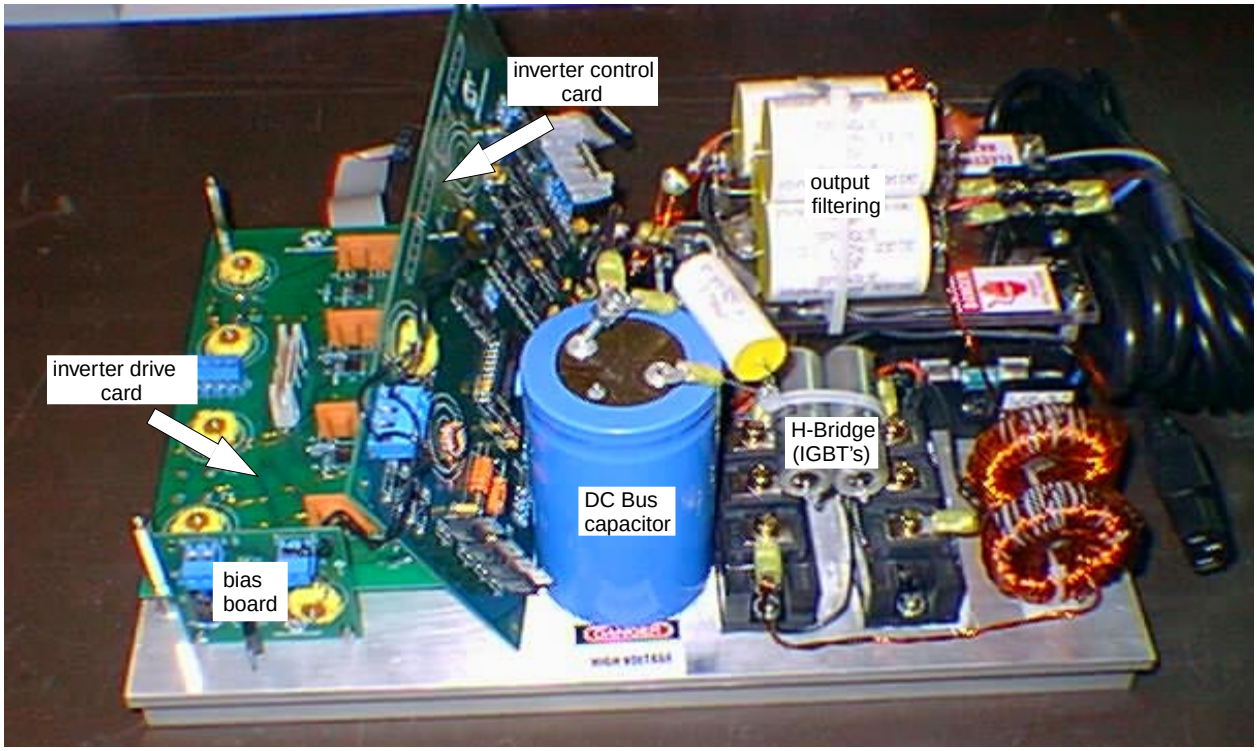
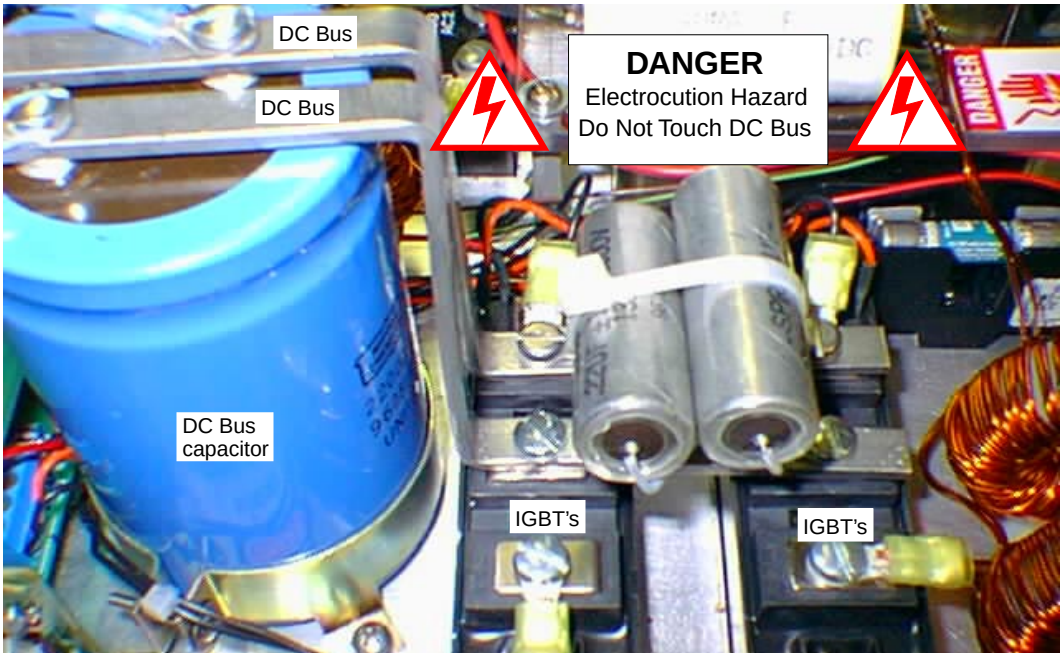


FIGURE F-9: DEMO FULL ASSEMBLY - DC BUS DETAIL



F.3 How to Demo the PICREF-1

DANGER

Electrocution Hazard
Do Not Disassemble Unit

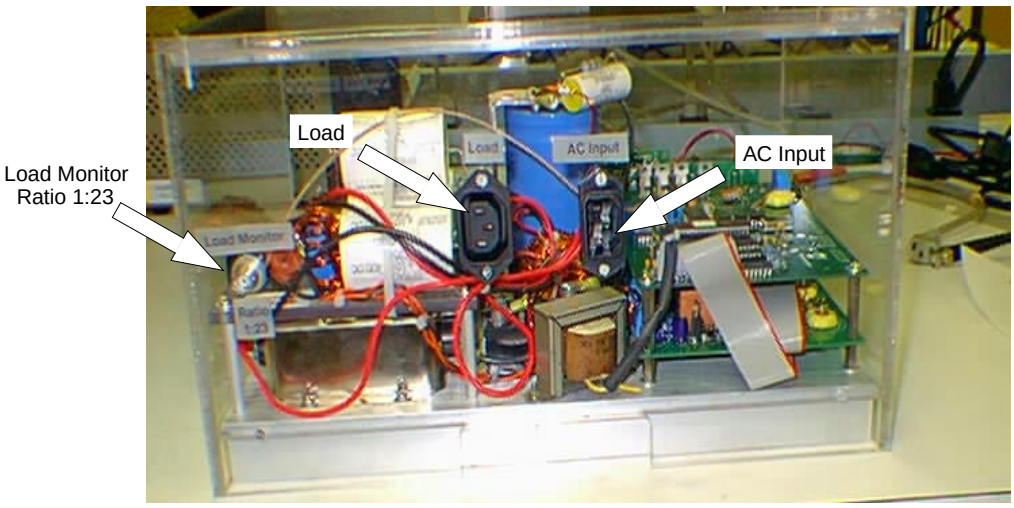
The UPS Demo Unit was not designed for sustained use, but only for short-term demonstration. Disconnect the unit when not in use.

Note:	An isolation transformer should be used with the UPS Demo Unit to avoid improper grounding.

Follow these steps to demo the UPS Demo Unit:

1. Plug the receptacle end of a power cord into the UPS Demo Unit “AC Input”. Plug the pronged end of the power cord into an AC wall socket.
2. Plug the load into the UPS Demo Unit “Load” socket (Optional). Make sure load can be driven by the UPS Demo.
3. Connect an oscilloscope probe to the UPS Demo Unit “Load Monitor” BNC connector.
4. Display (Stepped Down) AC Output waveform on oscilloscope.

FIGURE F-10: HOW TO SET UP DEMO UNIT - REAR VIEW



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